

Atomic layer etching removal of damaged layers in a contact hole for low sheet resistance

Jong Kyu Kim, Sung Il Cho, Sung Ho Lee, Chan Kyu Kim, Kyung Suk Min, and Geun Young Yeom

Citation: *Journal of Vacuum Science & Technology A* **31**, 061302 (2013); doi: 10.1116/1.4816321

View online: <http://dx.doi.org/10.1116/1.4816321>

View Table of Contents: <http://scitation.aip.org/content/avs/journal/jvsta/31/6?ver=pdfcov>

Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Instruments for advanced science

Gas Analysis



- dynamic measurement of reaction gas streams
- catalysis and thermal analysis
- molecular beam studies
- dissolved species probes
- fermentation, environmental and ecological studies

Surface Science



- UHV TPD
- SIMS
- end point detection in ion beam etch
- elemental imaging - surface mapping

Plasma Diagnostics



- plasma source characterization
- etch and deposition process reaction kinetic studies
- analysis of neutral and radical species

Vacuum Analysis



- partial pressure measurement and control of process gases
- reactive sputter process control
- vacuum diagnostics
- vacuum coating process monitoring

contact Hiden Analytical for further details

HIDEN
ANALYTICAL

info@hideninc.com
www.HidenAnalytical.com

CLICK to view our product catalogue



Atomic layer etching removal of damaged layers in a contact hole for low sheet resistance

Jong Kyu Kim,^{a)} Sung Il Cho, and Sung Ho Lee

Memory Division Semiconductor Business, Samsung Electronics, San No. 16 Banwol-Ri, Taejeon-Eup, Hwasung-City, Gyeonggi-Do, 449-711, South Korea

Chan Kyu Kim,^{a)} Kyung Suk Min, and Geun Young Yeom^{b)}

Department of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, Gyeonggi-Do 440-746, South Korea

(Received 20 January 2013; accepted 8 July 2013; published 26 July 2013)

A damaged layer remains on silicon substrates after high-aspect-ratio contact (HARC) etching when using a fluorocarbon gas. Atomic layer etching (ALET) is a technique that can be applied to remove the damaged layer of silicon, removing about 1.36 Å per etch cycle. The characteristics of contact damage removal by ALET are investigated and compared with the conventional damage removal technique of low-power CF₄ plasma etching. The low-power CF₄ plasma etching technique not only has inadequate etch depth control, but also introduces secondary damage by implanting impurities about 25 Å into the contact bottom of the silicon surface. However, ALET allows contact damage to be removed effectively without introducing secondary damage to the substrate, and with precision etch depth control at the angstrom scale. When ALET is applied subsequent to low-power CF₄ plasma etching, the fluorine- and carbon-damaged silicon is effectively removed in about 10 cycles. The sheet resistance of HARC etched silicon decreases from 142 to 137 Ω/□ after using low-power CF₄ plasma etching, and subsequent ALET treatment further decreases the sheet resistance to 129 Ω/□, which is close to the reference value of 124 Ω/□.

© 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4816321>]

I. INTRODUCTION

The critical lateral dimension of semiconductor devices has been reduced to less than 22 nm to obtain more devices capable of faster operation on the same silicon wafer. However, to maintain device properties, the vertical dimension of the device cannot be decreased proportional to the lateral dimension. For example, even though the capacitance required to operate a dynamic random access memory is not significantly decreased in devices with dimension less than 22 nm, the decrease of the lateral dimension reduces the operating capacitance by decreasing the total area of the capacitor structure. Therefore, to compensate for the decrease in area, the capacitor needs a cylindrical structure with a high aspect ratio and, additionally, an increased aspect ratio of the contact hole connecting the top and bottom structures of the capacitor.¹

To form a contact hole with a high aspect ratio, reactive ion etching with fluorocarbon-based gases is used. However, during the etching of the contact oxide, radiation damage to the contact hole occurs, including charge-up distortion, ion implantation, and fluorocarbon contamination.² As the aspect ratio of the contact hole is increased further with decreasing device size, higher ion energy bombardment is used to etch the contact hole to decrease distortion and increase its size. This further increases the damage at the bottom contact of the silicon.³ The presence of damage, fluorocarbon polymer residue, and implanted impurities such as carbon, fluorine, or oxygen on the silicon contact surface prevents the formation

of silicide and makes the electrical current flow difficult, thereby increasing sheet resistance.⁴ Increased sheet resistance decreases the device performance significantly and must be prevented.

A method used to prevent the increase of sheet resistance is the additional doping of the contact prior to contact oxide etching.⁵ This method is limited in its ability to decrease the sheet resistance, however, because the doping concentration is limited due to ion implantation. Even with increased doping concentrations, the damaged silicon prevents the effective formation of silicide. To remove the damaged layer, wet and dry etching methods have been investigated. Wet etching methods are found to successfully remove the damaged layer without forming secondary damage on the contact,⁶ but the uniformity and reliability of the etching cannot be easily controlled for high-aspect-ratio contacts (HARC), due to the difficulties in the chemical solution uniformly reaching the bottom of the contact. Also, due to the isotropic etching characteristics of wet chemical etching, the bottom contact of the silicon is etched isotropically without maintaining the vertical contact profile formed by the dry etching. This can create other problems, such as void formation and current leakage, to be induced on the contact during subsequent processes, such as contact metal deposition. Therefore, to remove the damaged contact bottom of the silicon layer, dry etching methods using plasmas are generally used.⁷

Low-power plasmas using fluorocarbon gases and hydrogen have been conventionally used to effectively remove the damaged contact of the silicon bottom.^{8–10} Low-power plasma etching techniques using fluorocarbon gases can also induce secondary damage on the silicon surface, although the

^{a)}Jong Kyu Kim and Chan Kyu Kim contributed equally to this work.

^{b)}Electronic mail: gyeoem@skku.edu

damage is not as heavy as that formed on the contact bottom after the contact oxide etching. This secondary damage on the silicon surface makes it more difficult to use the silicon for high aspect ratio contacts and for device structures that are sensitive to sheet resistance. The low ion mass of hydrogen plasma restricts secondary damage to the silicon surface. Also, the fluorocarbon polymer layer on the silicon surface can be effectively removed in the reaction with hydrogen without damaging the contact hole pattern structure due to hydrogen's extremely low reactivity with SiO_2 . However, because hydrogen also has a low reactivity with silicon, the damaged silicon layer is not easily removed.

Atomic layer etching (ALET) has recently been investigated as a possible next-generation etching technique. Like atomic layer deposition (ALD), ALET is a cyclic method. It involves the adsorption of one monolayer of reactive gas on the substrate, and the subsequent desorption of the reacted monolayer compound that forms on the substrate surface. During desorption, the surface compound layer alone is removed by supplying only enough energy to remove the top reacted monolayer without etching the unreacted underlying layer. Therefore, while ALD deposits one monolayer per cycle, ALET removes one monolayer per cycle. During the ALET desorption step, a particle bombardment energy range is chosen between that required for chemically enhanced ion etching (energetic neutral etching, in this case) and that for physical sputter etching in order to avoid sputtering the underlying layers after the top monolayer etching is complete. In this way, material can be precisely etched with atomic-scale depth control without causing damage to the substrate.¹¹

In this study, the characteristics of the contact bottom of the silicon layer after damage during the 20 nm-scale HARC etch processing are investigated using various methods, including simulation. We use ALET as a method to remove the damaged silicon layer, and its performance is compared with that of a conventional low-power plasma etching technique.

II. EXPERIMENT

Three hundred millimeter p-type (100) silicon wafers were etched using conventional HARC etch conditions with an overetching time of 20 s. The HARC etching was performed on a VIGUS instrument (Tokyo Electron Co. Ltd), which used a capacitively coupled plasma (CCP) of $\text{C}_4\text{F}_6/\text{O}_2/\text{Ar}$ at 15 mTorr, with 1500 W source power (W_s) and 7800 W bias power (W_b), where a bias voltage at 7800 W_b was about -4850 V. The fluorocarbon polymer layer remaining on the silicon wafer after the HARC etching was removed by applying oxygen plasma for 5 min [inductively coupled plasma (ICP), 13.56 MHz, 300 W_s , no bias power, and 10 mTorr O_2]. To remove the damaged silicon layer formed during the HARC etching, the silicon wafers were etched subsequent to the oxygen plasma cleaning by one or both of the two techniques. The first technique was a conventional low-power CF_4 plasma etch (ICP, 13.56 MHz, 300 W_s , 13.56 MHz, 300 W_b with a bias voltage at about -300 V, and 5 mTorr CF_4), and the second was ALET using Cl_2 gas.

The ALET etch technique is a cyclic process comprising four steps similar to those of the ALD technique, except that after one cycle of ALET, one monolayer is etched, while with ALD, one monolayer is deposited. Figure 1(a) shows a schematic drawing of the four process steps of ALET used in this experiment. During the first step, silicon chlorides are formed on the silicon surface by the Cl_2 gas flow (adsorption step). During the second step, the remaining Cl_2 gas is purged by evacuation. During the third step, the silicon chlorides formed on the silicon surface are preferentially removed using Ar particle bombardment (desorption step). During the fourth step, the etch byproducts are purged. For the adsorption step, 0.67 mTorr of Cl_2 was used because a pressure greater than 0.5 mTorr was required for adsorption. The use of higher pressures did not decrease the adsorption step time, which was instead found to be more dependent upon pressure stabilization. For the Ar particle bombardment during the desorption step, a three-grid ICP ion source was used (ICP, 13.56 MHz, 300 W, 20 sccm Ar) by applying 25 V to the extraction grid (energy control), -250 V to the acceleration grid (flux control), and 0 V to the ground grid (exit grid). To remove possible charge-related problems during ALET, parallel reflector plates with a 5° sloped angle were installed at the end of the ion gun. These low-angle reflectors formed a neutralized Ar particle beam by reflecting the Ar^+ ions extracted from the ion gun. Figure 1(b) shows a schematic of the ALET system with the neutral Ar beam source. Further details on the neutral beam source can be found elsewhere.¹²

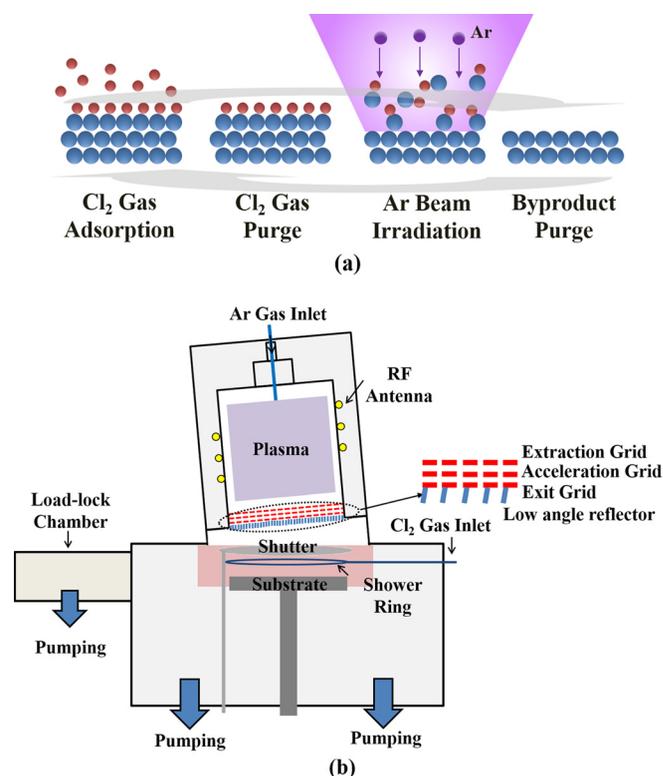


Fig. 1. (Color online) (a) Concept of the four-step ALET process and (b) schematic diagram of the ALET system using a three-grid ICP ion source with parallel reflectors.

To estimate the carbon penetration depth and the amount of fluorine remaining on the silicon surface after HARC and plasma etching, secondary ion mass spectroscopy (SIMS) was used (TOF-SIMS-5, sputtering with Cs^+ gun, analysis with Bi^+ gun), and the SIMS data were compared with Monte Carlo simulation data (Transport of Ions in Matter: TRIM). The silicon etch depth was measured using a surface profilometer (Tencor Instrument, Alpha Step 500), and the surface roughness on the etched silicon surface was measured by high-resolution atomic force microscopy (SII Nanotechnology, SPA-300HV). X-ray photoelectron spectroscopy (XPS, Thermo VG, MultiLab 200, Mg K α source) was used to estimate the surface contamination and binding states of surface components before and after the etching. The sheet resistances of the silicon surface were measured using a four-point probe after etching with HARC, low power CF_4 plasma, and ALET.

III. RESULTS AND DISCUSSION

To estimate the remaining silicon surface damage after HARC etching, the penetration depths of carbon and fluorine in the etched silicon surface were measured by SIMS and compared with the data obtained by the TRIM program (Fig. 2). Figure 2(a) shows the SIMS depth profiles of carbon and fluorine obtained on the p-type (100) silicon surface

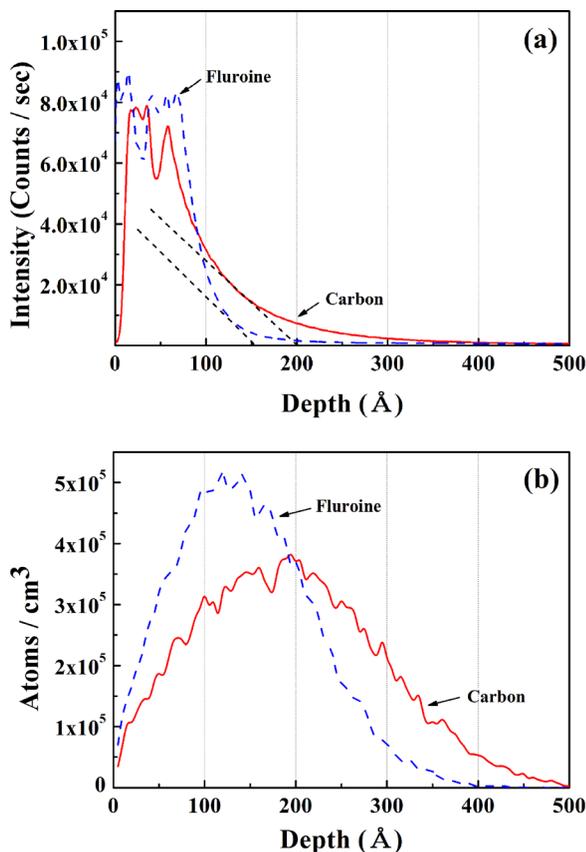


Fig. 2. (Color online) (a) SIMS depth profiles as a function of penetration depth (CCP, 1500 W_b , -4850 V , $\text{C}_4\text{F}_6/\text{O}_2/\text{Ar}$, 20 s) and (b) TRIM simulation data of carbon and fluorine ion distributions as a function of penetration depth (4850 eV).

after HARC etching for 20 s, and subsequent oxygen plasma cleaning for 5 min to remove the fluorocarbon polymer residue remaining on the etched silicon surface. The HARC etching time of 20 s is chosen by estimating the average time of the contact silicon surface exposure after cleaning the oxide in the contact hole. After the HARC etching and oxygen plasma cleaning, the penetration depths of carbon and fluorine are measured to be ≥ 200 and $\geq 150 \text{ \AA}$, respectively. This relatively large penetration depth into the silicon surface observed in the SIMS data is related to the high bias voltage condition of about -4850 V at 7800 W_b required to obtain a vertical contact hole during the HARC etching. For comparison, the penetration depths of carbon and fluorine into silicon are also estimated roughly using the TRIM program by setting the energy of carbon and fluorine at 4850 eV [Fig. 2(b)]. In the TRIM data, the penetration depths of carbon and fluorine show a Gaussian distribution with a maxima at about 200 and 150 \AA , respectively, due to the assumption in the calculation of monoenergetic ions. In the SIMS data, the peak concentrations of carbon and fluorine are very near the surface due to the multiple contributions from the energy distribution of the ions bombarding the silicon surface, molecular ions such as C_xF_y^+ , carbon and fluorine, and the continuous etching of the silicon surface. However, the TRIM simulation is similar to the SIMS data in the prediction that carbon penetrates further than fluorine, with a penetration depth of $\geq 200 \text{ \AA}$. Therefore, the severely damaged contact silicon layer can be estimated to be at least 200 \AA deep for the HARC etching conditions used in this experiment.

The 200 \AA -deep heavily damaged silicon layers should be removed using a separate silicon etching method, and a widely used method is low-power CF_4 plasma etching. To remove the damaged layer, the silicon is exposed to the plasma for 5 s with an etch rate of about 40–50 $\text{ \AA}/\text{s}$. In addition, a -300 V bias voltage is required to etch the damaged silicon surface deep in the contact hole, though the use of this bias voltage can generate secondary damage on the silicon surface. Figures 3(a) and 3(b) show the SIMS depth profiles of carbon and fluorine measured after etching a reference silicon wafer using low-power CF_4 plasma etching. The penetration depth profiles into the silicon are estimated using the TRIM program with an assumed particle energy of 300 eV. An undamaged reference silicon wafer is also used in the experiment to more clearly evaluate the secondary silicon surface damage caused by the low-power CF_4 plasma etching. As shown in Fig. 3(a), the penetration depths of carbon and fluorine are about 25 \AA , which is much less than those observed after HARC etching. The concentration of fluorine in the silicon is much higher than carbon, possibly due to the low C/F ratio of the low-power CF_4 plasma etching conditions. In the TRIM results, penetration peaks for carbon and fluorine near 20 \AA are also observed [Fig. 3(b)]. It is likely, therefore, that even after removing the heavily damaged HARC-etched silicon layer using conventional low-power CF_4 plasma etching, secondary damage remains at a depth of about 25 \AA , and this damage may affect the electrical properties of the contact.

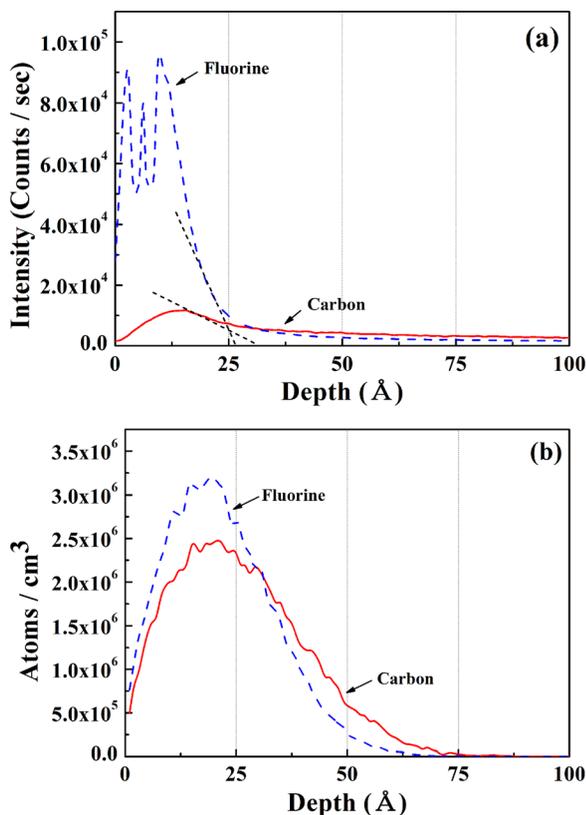


Fig. 3. (Color online) (a) SIMS depth profiles of carbon and fluorine after reference silicon wafer etching using low-power CF_4 plasma etching conditions (ICP, 13.56 MHz, 300 W_s, -300 V, CF_4 , 5 s) and (b) TRIM simulation data of carbon and fluorine ion distributions as a function of penetration depth (300 eV).

Using XPS, the surface binding states of the silicon with fluorine and carbon immediately after the HARC etching (i) and after subsequent oxygen plasma cleaning (ii) are investigated. The XPS narrow scan data are shown in Figs. 4(a) and 4(b). The XPS narrow scan data for fluorine and carbon on unetched silicon (iii) are also included in all plots as a reference. As shown in Fig. 4(a), O-F and C-F bonds are observed after the HARC etching, possibly due to the formation of a polymer layer on the silicon surface as a result of using $\text{C}_4\text{F}_6/\text{O}_2/\text{Ar}$ during etching. After oxygen plasma cleaning, the bonding state of fluorine is changed to Si-F, which indicates removal of the polymer and exposure of the remaining damage on the silicon surface. In Figure 4(b), the carbon binding peaks after HARC etching show bonds such as C-CF, C-O, and C-F, which are all due to the etch chemistry. After oxygen plasma etching, a Si-C bonding peak indicates damage on the silicon surface, and the presence of a C-C bonding peak is observed that is similar to the reference spectra. The appearance of Si-F and Si-C silicon bonding appears to be related to the penetration of carbon and fluorine into the silicon surface. This penetration damages the silicon surface and increases the silicon sheet resistance by preventing the formation of contact silicide during the subsequent processing steps.

As a possible method to remove the damaged silicon surface layer with precise control and without secondary damage, silicon ALET is investigated. The advantage of ALET is

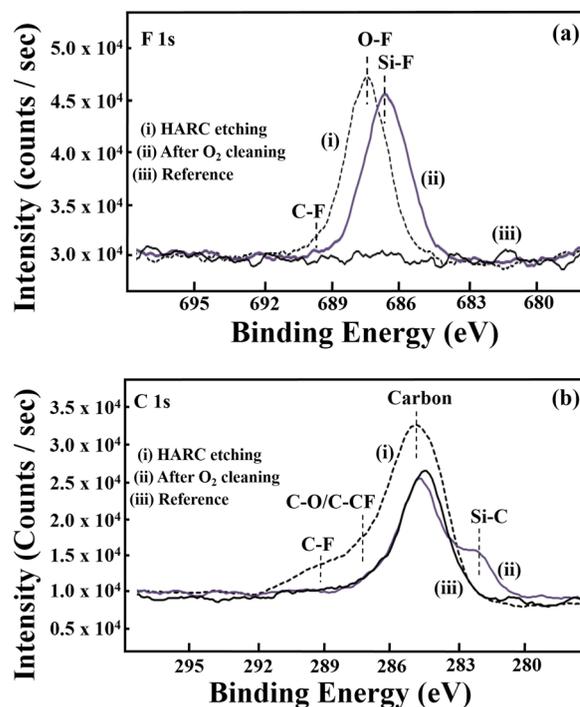


Fig. 4. (Color online) XPS narrow scan spectra of (a) fluorine and (b) carbon after HARC etching (i), after polymer residue removal by oxygen plasma cleaning subsequent to HARC etching (ii), (ICP, 13.56 MHz, 300 W_s, No Bias, O_2 , 5 min), and for reference silicon (iii).

that this technique can remove one monolayer per etch cycle, but to do so the silicon surface must be fully covered with Cl_2 by supplying enough Cl_2 gas flow during the adsorption step. In addition, all of the silicon chlorides formed on the silicon surface must be removed without sputtering the underlying silicon layer during the desorption step. To provide full coverage of Cl_2 on the silicon surface during the adsorption step, a Cl_2 pressure of 0.67 mTorr is supplied for 20 s. To determine the Ar neutral beam dose required to remove all the silicon chlorides formed on the silicon surface, the Ar beam irradiation time was varied from 0 to 200 s while maintaining the energy of the Ar^+ ion gun at +25 V (acceleration grid voltage). This particular voltage is chosen for the Ar^+ ion gun so the underlying silicon layer is not sputtered after removal of the top silicon chlorides. Detailed operating conditions are found in Table I. Figure 5(a) shows the etch rate

TABLE I. Typical experimental parameters of ALET in this work.

Parameter	Value
Base pressure	5.0×10^{-7} Torr
Working pressure	7.0×10^{-5} Torr
Inductive power	300 W
Acceleration grid voltage	25 V
Focusing grid voltage	-250 V
Ar irradiation time	~0–200 s
Ar gas flow rate	20 sccm
Cl_2 pressure	0.67 mTorr
Cl_2 supply time	20 s
Substrate temp.	RT
Number of cycle	~50–200 cycles

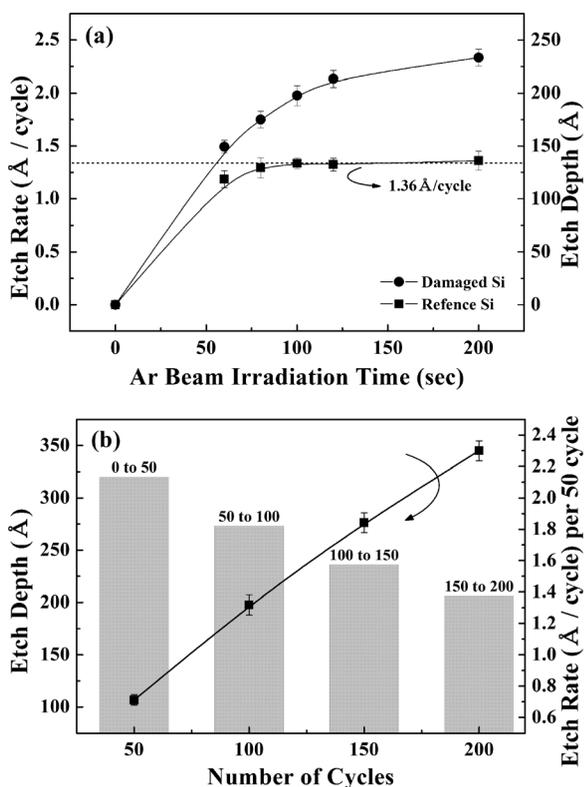


Fig. 5. (a) Silicon etch rate ($\text{\AA}/\text{cycle}$) and total etch depth as a function of Ar beam irradiation time for the reference (100) silicon and the (100) silicon damaged by HARC etching (subsequent to oxygen plasma cleaning). (b) The silicon etch depth and etch rate calculated in 50 cycle increments while keeping the Ar beam irradiation time at 100 s, thereby measuring the average etch rate at a particular silicon depth range.

of silicon ($\text{\AA}/\text{cycle}$) measured as a function of the Ar beam irradiation time for the reference (100) silicon and the (100) silicon damaged by the HARC etching (and subsequent oxygen plasma cleaning). The etch rate is calculated by measuring the silicon etch depth (\AA) after 100 etching cycles and dividing this etch depth by the number of etch cycles. The silicon etch rate for the reference silicon sample is initially low, but then increases with the Ar beam irradiation time due to the increased removal of silicon chloride per cycle. For an Ar beam irradiation time greater than 100 s, the silicon etch rate is saturated at $1.36 \text{\AA}/\text{cycle}$. This indicates that the underlying silicon layer is now exposed due to the one-monolayer etching per cycle, and that all of the silicon chloride formed on the silicon surface has been removed without further sputtering. However, for silicon damaged by HARC etching (and subsequent oxygen plasma cleaning), the same Ar beam irradiation time results in a silicon etch rate that is higher and not completely saturated until the Ar beam irradiation time is increased to 200 s. This higher silicon etch rate with the same Ar irradiation time and without saturation is due to the lower silicon bonding energy on the damaged silicon surface compared to that of the reference silicon, due to bonding with carbon and fluorine and defects in the silicon lattice.

The damage on the silicon surface created by HARC etching is limited to the layers near the surface, and as the etch depth increases, the damage is expected to decrease

[Fig. 5(a)]. Therefore, the silicon damaged by HARC etching is etched with ALET for 200 cycles, measuring the etch rate every 50 cycles while maintaining the 100 s Ar beam irradiation time. This enables measurement of the average etch rate at a particular silicon depth range, and the results are shown in Fig. 5(b). For the first 50 cycles, the average etch rate is as high as $2.13 \text{\AA}/\text{cycle}$ due to the severe lattice defects and heavy bonding to carbon and fluorine at the silicon surface. However, as the number of etch cycles increases and the average etch rate is measured at deeper locations in the silicon, the silicon etch rate decreases. Eventually, when the silicon etch depth reaches levels greater than 250\AA , an etch rate of $1.37 \text{\AA}/\text{cycle}$, close to that of the reference silicon, is observed due to the complete removal of silicon damage.

Based on these results, the silicon surface damaged by HARC etching (and subsequent oxygen plasma cleaning) is etched with ALET for 100 cycles, while bombarding for 100 s of Ar during the desorption. This etching removes about 200\AA of material due to the higher silicon etch rate for damaged silicon, as shown in Fig. 4(a). The XPS narrow scan data of carbon and fluorine on the silicon etched by ALET are measured and compared with those measured after etching using low-power CF_4 plasma for about 200\AA . The results are shown in Figs. 6(a) and 6(b) for fluorine and carbon, respectively. It is easy to control the ALET etch depth to 200\AA by controlling the number of etch cycles, even though the etch rate is not completely saturated. Due to the difficulty of precisely controlling the etch depth of low-power CF_4 plasma etching, the etch depth is only specified in a range of $\sim 200\text{--}250 \text{\AA}$. As shown in Fig. 6(a), after 100

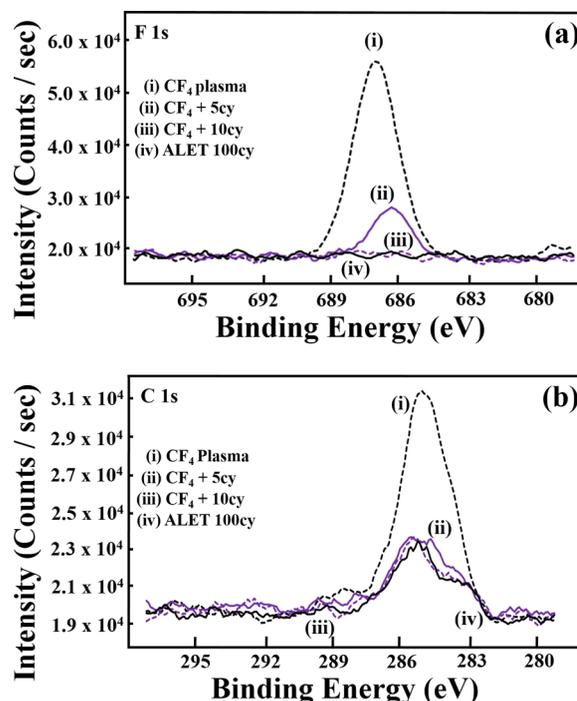


Fig. 6. (Color online) XPS narrow scan spectra of (a) fluorine and (b) carbon after removal of the damaged layer by low-power CF_4 plasma etching (i) (ICP, 13.56 MHz, 300 W_{st}, -300 V , CF_4 , 5 s), after low-power CF_4 plasma + 5 ALET cycles (ii), after low-power CF_4 plasma + 10 ALET cycles (iii) and after 100 ALET cycles only (iv).

cycles of ALET on the silicon damaged by HARC etching (iv), no trace of fluorine can be found. However, a fluorine peak related to the Si–F bonding is found on the silicon surface after low-power CF_4 plasma etching (i), possibly due to the secondary damage observed in Fig. 3(b), even though most of the HARC etching damage layers are removed. Comparable to the fluorine results, a higher carbon bonding peak related to Si–C bonding is observed after low-power CF_4 plasma etching, and a carbon peak height similar to that of the reference silicon is observed after 100 cycles of ALET [Fig. 6(b)]. Therefore, it can be concluded that ALET can effectively remove the HARC etching damage layer with precise etch depth control and without causing secondary damage.

In general, ALET is a slow process, and removing a 200 Å-thick damaged silicon layer would be time-consuming. Therefore, a combination of low-power CF plasma etching and ALET is investigated to practically remove a silicon layer damaged by HARC etching. Figures 6(a) and 6(b) also show the XPS narrow scan data of fluorine and carbon, respectively, after the combinations of low-power CF_4 plasma etching and 5 ALET cycles (ii), and after low-power CF_4 plasma etching and 10 ALET cycles (iii). More than 20 min is still required for etching 10 ALET cycles using the current ALET equipment. However, the ALET process time may be decreased considerably by using a higher Cl_2 pressure and a higher flux plasma source for a shorter adsorption/desorption time. A small fluorine peak can still be observed after the combination etching using five ALET cycles (ii), indicating that the secondary damage has not been fully removed. However, after the combination etching using 10 ALET cycles (iii), the fluorine peak is completely removed and the data appears to be similar to the data for 100 ALET cycles (iv). For carbon, the combination etching using 10 ALET cycles leaves a very small carbon peak related to Si–C bonding, but the peak height is negligibly small. Therefore, it is reasonable to assume that the silicon damage created by HARC etching is effectively and efficiently removed using a combination of low-power CF_4 plasma etching and 10 ALET cycles.

The root-mean-square (RMS) surface roughness (measured using AFM) and the sheet resistance (measured using a four-point probe) of the silicon surface are shown in Figs. 7(a) and 7(b), respectively, for the five sample etching conditions used in this work. The first etching condition is the silicon surface immediately after the initial HARC etching (and subsequent oxygen plasma cleaning), and the other four etching conditions are subsequent to HARC: namely, after low-power plasma CF_4 plasma etching, after the combination etching of low-power plasma CF_4 plasma etching plus five ALET cycles, after the combination etching of low-power plasma CF_4 plasma etching plus 10 ALET cycles, and 100 ALET cycles only. The RMS and sheet resistance measurements of the reference silicon are also shown. As shown in Figure 7(a), after HARC etching, the roughness is significantly increased from 3.48 to 36.26 Å, possibly due to the formation of micromasking by the polymer layer during the etching step using $\text{C}_4\text{F}_6/\text{O}_2/\text{Ar}$. After removing the damaged

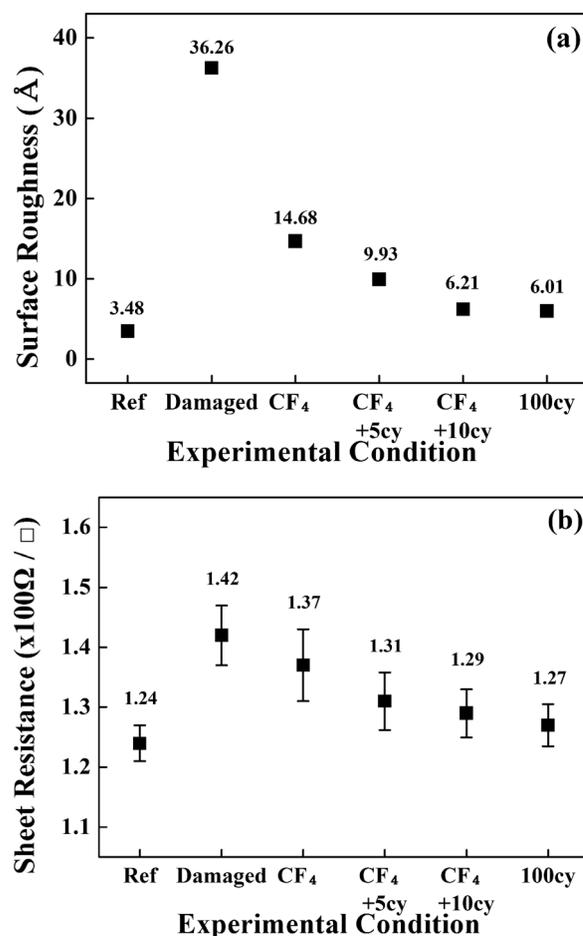


Fig. 7. (a) RMS surface roughness and (b) sheet resistance of the silicon surface for the reference silicon surface (i), and after HARC etching (subsequent to oxygen plasma cleaning) (ii). Also plotted are the measurements after damaged HARC layer removal using low-power CF_4 plasma etching (iii), low-power CF_4 plasma + 5 ALET cycles (iv), low-power CF_4 plasma + 10 ALET cycles (v), and 100 cycles of ALET.

silicon layer using low-power CF_4 plasma etching, the surface roughness decreases to 14.68 Å. The lowest surface roughness found on samples that have been initially etched using HARC is an RMS of 6.01 Å, and occurs after 100 ALET cycles. This low surface roughness is related to the removal of a uniform surface layer during each cycle of the ALET, which decreases the pillar height with the increase of etch depth. In the combination etching steps which add 5 and 10 ALET cycles after low-power CF_4 plasma etching, the surface roughness decreases to 9.93 and 6.21 Å, respectively. Therefore, the surface roughness of the combination etching after the 10 ALET cycles is similar to that of 100 ALET cycles.

The sheet resistances measured using the four-point probe, shown in Fig. 7(b), reveals a trend similar to that of the surface roughness. It is known that a higher contact silicon surface roughness increases the sheet resistance and prevents the effective formation of silicide on the contact during subsequent processes. Therefore, the sheet resistance can be further increased after the formation of silicide. The change of the sheet resistance as a function of processing conditions is believed to be partially related to the change of the surface roughness, and partially related to the remaining

impurities, such as carbon and fluorine, and lattice defects in the silicon. After HARC etching (and subsequent oxygen plasma cleaning), the sheet resistance increases by about 15% from 124 to 142 Ω/\square . However, after low-power CF_4 plasma etching the sheet resistance decreases to 137 Ω/\square , and after 100 ALET cycles the sheet resistance decreases to 127 Ω/\square , which is similar to the reference value. Using the combination etching of low-power CF_4 plasma etching plus 10 ALET cycles, a sheet resistance of 129 Ω/\square can be obtained. Therefore, the combination of low-power CF_4 plasma etching and 10 ALET cycles effectively and efficiently removes the silicon contact damage caused by HARC etching, enabling us to obtain surface conditions similar to those of the reference sample.

IV. SUMMARY AND CONCLUSIONS

As the critical dimension of semiconductor devices is reduced to less than 22 nm, samples need to be etched using a high-bias reactive ion etching technique using fluorocarbon-based gases. During this etching, the contact silicon is damaged and the device characteristics can be degraded. In this study, the characteristics of the contact silicon damage formed after HARC etching are investigated, and effective methods are examined to remove the contact silicon damage. It is found that the silicon contact damage layer after conventional HARC etching can be ≥ 200 Å-thick, and is created due to the penetration of carbon and fluorine and by the formation of binding states such as Si–F and Si–C in addition to lattice damage. When a conventional low-power CF_4 plasma etching technique is used to remove the damaged silicon contact layer, secondary silicon surface damage penetrating about 25 Å into the material remains, even though the HARC etching damage layer is completely removed. By using silicon ALET subsequent to HARC etching, one silicon monolayer

per etch cycle (1.36 Å/cycle) is removed with no secondary damage, and the electrical, physical, and chemical properties of the silicon approach close to those of the unetched silicon surface. In addition, ALET allows the etch depth into the silicon surface to be precisely controlled. By combining low-power CF_4 plasma etching with 10 ALET cycles, the properties of the damaged contact silicon such as the sheet resistance and surface roughness are recovered to levels similar to those obtained after 100 ALET cycles. This is because the secondary damage created during the combination etching by the low-power CF_4 plasma etching step is removed during the 10 ALET cycles.

ACKNOWLEDGMENT

This work was supported by the World Class University Program of the National Research Foundation of Korea (Grant No. R32-10124).

- ¹T. Yamada, S. Samata, H. Takato, Y. Matsushita, K. Hieda, A. Nitayama, F. Horiguchi, and F. Masuoka, *IEEE Trans. Electron Dev.* **38**, 2481 (1991).
- ²T. Goto, H. Yamauchi, T. Kato, M. Terasaki, A. Teramoto, M. Hirayama, S. Sugawa, and T. Ohmi, *Jpn. J. Appl. Phys.* **43**, 1784 (2004).
- ³M. Wang and M. J. Kushner, *J. Vac. Sci. Technol. A* **29**, 051306 (2011).
- ⁴H. S. Lee, K. S. Shin, N. M. Cho, G. J. Min, C. J. Kang, W. S. Han, and J. T. Moon, *Thin Solid Films* **517**, 3844 (2009).
- ⁵M. A. Khan, M. S. Shur, and Q. Chen, *Appl. Phys. Lett.* **68**, 3022 (1996).
- ⁶M. Miyamoto, N. Kita, S. Ishida, and T. Tatsuno, *J. Electrochem. Soc.* **141**, 2899 (1994).
- ⁷S. J. Fonash, *J. Electrochem. Soc.* **137**, 3885 (1990).
- ⁸M. A. Foad, S. Thoms, and C. D. W. Wilkinson, *J. Vac. Sci. Technol. B* **11**, 20 (1993).
- ⁹G. S. Oehrlein, *Mater. Sci. Eng. B* **4**, 441 (1989).
- ¹⁰N. Akira, A. Yasushi, U. Yukihiro, H. Kenji, S. Yasumasa, and S. Masakazu, *Jpn. J. Appl. Phys.* **36**, 3639 (1997).
- ¹¹C. K. Oh, S. D. Park, H. C. Lee, J. W. Bae, and G. Y. Yeom, *Electrochem. Solid-State Lett.* **10**, H94 (2007).
- ¹²B. J. Park *et al.*, *J. Phys. D: Appl. Phys.* **41**, 024005 (2008).