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Damaged silicon contact layer removal using atomic layer etching for deep-nanoscale semiconductor devices

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Silicon atomic layer etching (ALET) using Cl_2 is applied to remove the damaged layer on a 30 nm contact silicon surface formed by high-energy reactive ions during high aspect ratio contact etching, and its effects on the damage removal characteristics are investigated. Compared to a conventional damage removal method, such as the low-power CF_4 plasma treatment technique, ALET produces less secondary damage to the substrate and gives exact etch depth control and extremely high etch selectivity to the contact SiO_2 insulating pattern mold. When ALET is applied after a conventional damage removal technique, the sheet resistance of the damaged contact silicon surface is improved to a level close to that of a clean silicon surface, while exact atomic-scale depth control is maintained without changes in the pattern mold profile. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4823335]

I. INTRODUCTION

With the design rule of semiconductor devices promoting shrinkage, the pattern width of the semiconductor device circuit is decreasing while the thickness of the layer is maintained. As a result, the aspect ratio of the pattern is significantly increased. To effectively form fine patterns with a high aspect ratio on the semiconductor contact during reactive ion etching, a plasma processing technique using reactive ions with higher energies has been utilized called high aspect ratio contact (HARC) etching.[1] Although high-energy reactive ions during HARC etching can produce fine, vertical contact patterns, they also physically damage and contaminate the contact silicon surface.[2] The physical damage of the silicon lattice atoms caused by the high-energy ion bombardment disturbs electron transport and increases the contact surface resistance. In addition, contamination and implantation on the contact silicon surface by the etchant species, such as fluorine and carbon, prevent reactions between Si and Ti or Co, which are deposited on the silicon contact surface to act as a conducting metal to achieve low contact resistance.

Figure 1 shows the cross-sectional transmission electron microscope (TEM) images of the Ti silicide contacts formed on an undamaged contact surface for a shallow contact [Fig. 1(a)] and formed on a damaged/contaminated contact surface after silicidation [Fig. 1(b)], respectively. When a contact surface is damaged or contaminated because of nonuniform and insufficient silicidation on the contact surface of the deposited Ti, as shown in Fig. 1(b), it is difficult to form an Ohmic contact, and therefore, the contact resistance is increased.[3] The drastic shrinkage pursued by the progressive design rule necessitates the use of higher energy reactive ions for effective etching of the HARC oxide, which tends to increase the damage of the silicon surface on the contact bottom.[4]

Various methods have been investigated to eliminate the damage formed on the contact silicon surface. One approach is to decrease the silicon damage during the plasma processing itself by decreasing the high-energy ion bombardment on the contact silicon surface.[5] However, decreasing the reactive ion energy can degrade the precise HARC patterning required by the design rule, which is generally obtained at high reactive ion energy conditions. Therefore, with the shrinkage required by the design rule, it has become more difficult to find a process window for optimum HARC patterning using low reactive ion energy. In addition, the use of lower reactive ion energy during HARC etching does not guarantee an undamaged contact silicon surface, so this approach may not be applicable for next-generation devices which require significantly lower contact resistances.

Another approach to eliminate surface damage is to effectively remove the damaged layer caused by HARC etching.[6,7] One method used to remove the damaged silicon layer is the wet chemical etching method.[7,8] However, this method cannot be applied when the contact size is tens of nanometers or less because of the difficulty in cleaning a deep contact with wet chemicals and the limited etch depth and width control, although this method has been successfully applied in cleaning larger contact sizes. The method most commonly used to remove the damaged layer is low-energy plasma treatment.[9] Low energy fluorine-based ions generated by a plasma at low pressure are used to remove

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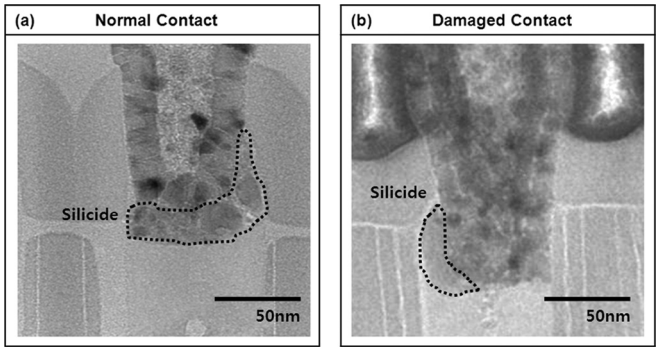

FIG. 1. TEM cross-sectional images of the silicon contact after Ti silicidation for (a) a normal contact and (b) a damaged contact (HARC).

the damaged silicon layer on the contact bottom surface.[9] Figure 2 shows the resistance of the damaged/contaminated contact in Fig. 1(c) after the damaged layer was removed using the low pressure CF_4 plasma treatment for different plasma treatment times. The process conditions for this treatment are described in Sec. II. Contact resistance is measured with a direct contact (DC) pattern in 20-nm-scale dynamic random access memory (2X DRAM) devices. As shown in Fig. 2, the removal of the damaged layer by CF_4 plasma treatment using low-energy reactive ions decreased the contact resistance by about 24%. However, low-energy CF_4 plasma treatment can induce secondary damage on the contact surface, and the evidence of this can be seen in Fig. 2 for longer plasma treatment times. When plasma treatment is continued up to 45 s, the contact resistance increases only slightly possibly due to the secondary damage of the contact surface by the reactive ion bombardment during CF_4 plasma treatment. In addition, during low-energy CF_4 plasma treatment, the SiO_2 contact hole pattern can be deformed due to the lack of etch selectivity with SiO_2, and the exact contact silicon etch depth is difficult to control.[10]

Therefore, other methods which can remove the damaged contact silicon layer without inducing secondary damage on the contact silicon surface and without degrading the SiO_2 contact hole pattern profile while enabling control of the exact etch depth have been investigated.[11,12] The most promising methods use hydrogen plasma or atomic layer etching

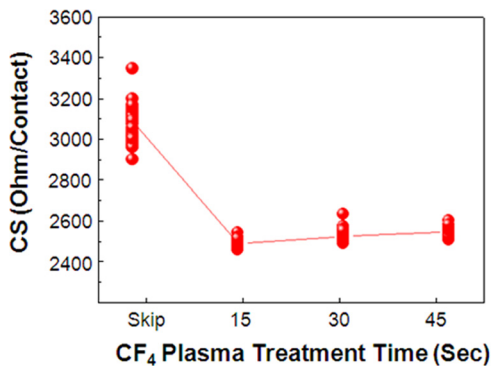

FIG. 2. (Color online) Resistances of the contacts in Fig. 1 after the removal of the damage using the low-energy CF_4 plasma treatment for different plasma treatment times. The contact resistance is measured with a DC pattern in 2X DRAM devices.

(ALET). For the hydrogen plasma methods, because of the low reactivity of hydrogen with SiO_2 and the low mass of the hydrogen atom, we can expect very little degradation of the SiO_2 contact hole profile and very little physical damage on the contact silicon surface, with the additional benefit of carbon-related species removal from the contact silicon surface.[11] In general, however, hydrogen plasma methods have difficulty in removing the damaged silicon layer due to the low reactivity of the hydrogen atom with silicon, even though specific plasma sources, such as the electron cyclotron plasma source, have been reported to give some moderate silicon etch rates.[13]

Recently, we introduced the silicon ALET using Cl_2 as an efficient method for removing damaged silicon layers formed after HARC etching on blank silicon wafers.[12] The ALET method is a cyclic etch method wherein chlorine atoms are adsorbed on the silicon layer during the Cl_2 adsorption step, and the chemisorbed silicon layer is removed by a controlled low-energy Ar beam during the desorption step.[14] By repeating the adsorption step and the desorption step, exactly one silicon monolayer can be removed during each cycle without damaging the underlayer.[15–17] In our study, the removal of the damaged silicon layer from a 30 nm HARC pattern by ALET was investigated and compared with that by the conventional low-energy CF_4 plasma treatment technique.

II. EXPERIMENT

The wafers used in this experiment were fabricated by depositing 200-nm-thick layers of SiO_2 using tetraethyl orthosilicate (TEOS) on p-type Si (100) wafers, respectively. For 30 nm HARC patterning, 100-nm-thick amorphous carbon layers (ACL) were deposited on the SiO_2, and the ACL layers were patterned as a hardmask using 30 nm of contact photoresist. The TEOS oxide wafer with the ACL mask was etched using a commercial capacitively coupled plasma (CCP) etcher with a HARC etch recipe [100 sccm C_4F_6/10 sccm O_2/100 sccm Ar, a pressure of 15 mTorr, a source power (W_s) of 1500 W_s, and a bias power (W_b) of 7800 W_b] at the 30% overetch condition. After completion of the HARC etching, a fluorocarbon polymer layer was formed on the contact by inductively coupled plasma processing (ICP, 13.56 MH_z 300 W_s, no bias power, 10 mTorr O_2) for 5 min. After oxygen ICP cleaning, the damaged silicon layer formed on the contact bottom surface during HARC etching was removed by the ALET method using Cl_2 gas and by the conventional low-power CF_4 plasma etching technique (ICP, 13.56 MH_z 1300 W_s, 13.56 MH_z 300 W_b; bias voltage approximately −300 V, 5 mTorr). Low-power CF_4 plasma etching is one of the actual contact damage removal processes used on 2X DRAM devices.

The schematic diagram of the ALET system used in this experiment is shown in Fig. 3, and the process conditions are shown in Table I. The ALET source was a neutral beam source composed of a three-grid ICP-type ion gun (13.56 MH_z 300 W, 20 sccm Ar), which extracts the Ar ion beam, and a low angle reflector, which neutralizes the extracted Ar ion beam. The Ar ion beam was neutralized in this experiment

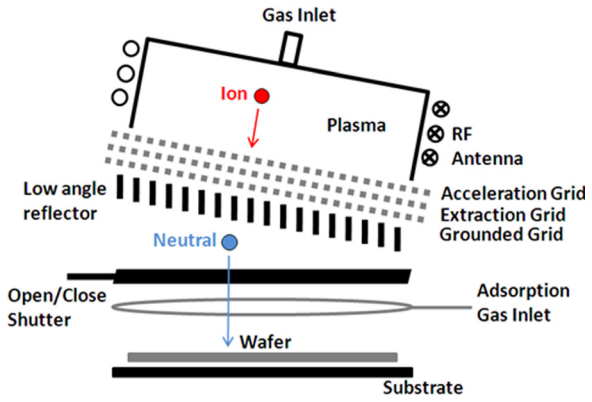

FIG. 3. (Color online) Schematic diagram of the ALET source composed of a three-grid ICP ion gun and a low-angle reflector.

to remove possible problems related to the charging of the HARC hole during ALET. The energy of the extracted Ar ion beam was controlled by the voltage applied to the extraction grid, while the acceleration grid controlled the beam flux. The detailed process of ALET is shown in Fig. 4 schematically. To adsorb the Cl_2 onto one silicon monolayer, 0.67 mTorr of Cl_2 gas was maintained for 20 s. For the desorption of the Cl_2 chemisorbed silicon layer, the Ar beam from the ALET source was irradiated onto the acceleration grid (first grid) for 100 s at +25 V, which prevented sputtering of the exposed underlayer after the removal of the top chemisorbed silicon layer, and onto the extraction grid (second grid) at −250 V. The last grid (third grid) was grounded so that the energy of the ions passing through it would correspond to the acceleration grid voltage and would not form into a plasma in the processing chamber. The remaining gases and byproducts were purged between the adsorption and desorption steps by bringing the chamber to vacuum. After one cycle, exactly one silicon monolayer was removed.[13–15]

To estimate the damage and contamination on the contact bottom silicon surface after HARC etching and after the subsequent plasma processing, the SiO_2 patterning mold was selectively removed via HF solution (H_2O:HF = 8:1), which exposed the contact bottom silicon. As a reference, nonpatterned blank 200-nm-thick SiO_2-covered silicon wafers were also HARC-etched, and their surface characteristics were compared with those of the patterned wafers. The penetration depths of carbon and fluorine into the contact bottom silicon surface after HARC etching were estimated by secondary ion mass spectroscopy (SIMS, sputtering with Cs^+ gun). X-ray photoelectron spectroscopy (XPS, Thermo VG, MultiLab 200, Mg Kα source) was used to estimate the degree of surface contamination caused by the remaining fluorine and carbon on the contact bottom silicon surface before and after the etching. The change in the SiO_2 contact hole profile after the HARC etching and subsequent plasma processing were observed by scanning electron microscopy (SEM). The sheet resistance of the silicon surface exposed after the removal of SiO_2 mold was measured using a four point probe (Keithley Instrument, Model 2000) and used as an estimate of the contact resistance.

TABLE I. Typical experimental parameters of ALET used in this work.

Parameter	Value
Base pressure	5.0×10^{-7} Torr
Working pressure	7.0×10^{-5} Torr
Inductive power	300 W
Acceleration grid voltage	25 V
Extraction grid voltage	250 V
Ar irradiation time	100 s
Ar gas flow rate	20 sccm
Cl_2 pressure	0.67 mTorr
Cl_2 supply time	20 s
Substrate temperature	RT

III. RESULTS AND DISCUSSION

Figure 5(a) shows the 30 nm contact SiO_2 etch profile observed by SEM after HARC etching using ACL as the etch mask, and Fig. 5(b) shows the contact SiO_2 etch profile after oxygen plasma etching. A polymer layer was initially observed at the contact bottom area, but after the oxygen plasma etching, the polymer layer as well as the ACL mask was removed [Fig. 5(b)]. However, the silicon layer at the bottom of the contact damaged during HARC etching was still present. To investigate the characteristics of the damaged contact silicon surface, the contact SiO_2 mold layer was etched selectively using HF solution to expose the contact bottom silicon, and this etched layer is shown in Fig. 5(c). After the removal of the SiO_2 contact mold layer in the stage of Fig. 5(b) via HF solution, the damaged silicon layer at the contact bottom was exposed without changes of the recess shape and depth of the contact bottom silicon surface.

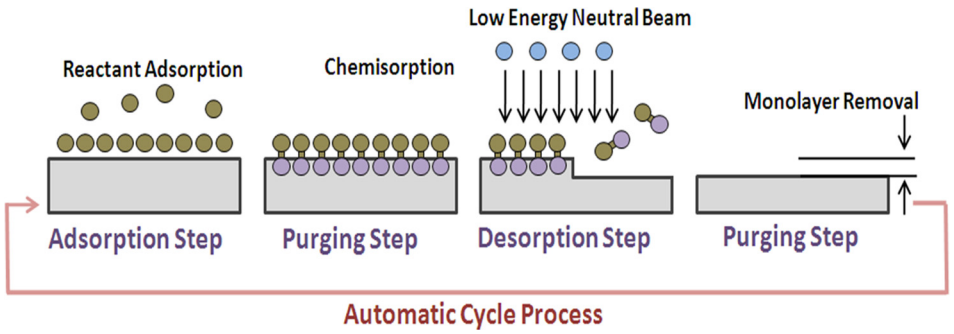

FIG. 4. (Color online) Process concept of silicon ALET using Cl_2.

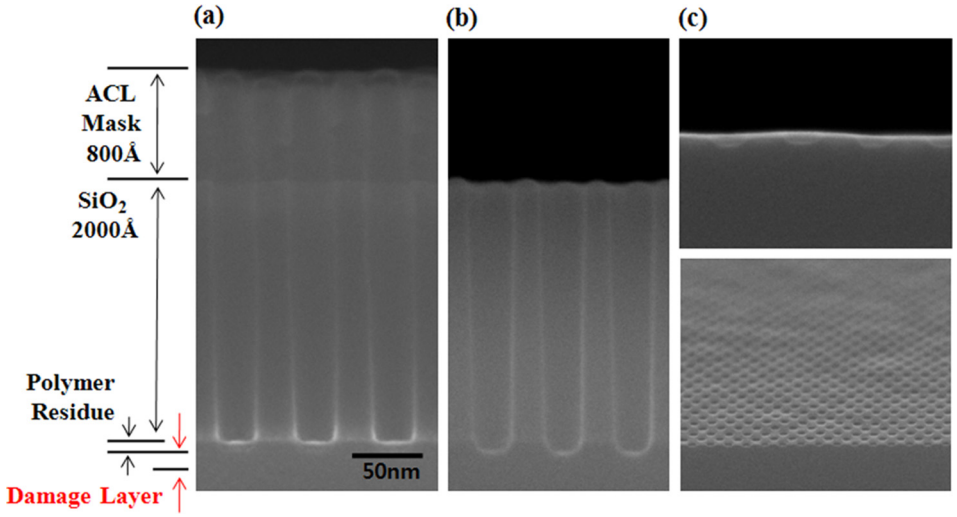

FIG. 5. (Color online) SEM image of the 30 nm contact (a) after the HARC etching, (b) after polymer removal by O_2 plasma treatment, and (c) after SiO_2 removal using an HF solution.

The exposed contact silicon surface was investigated using XPS to determine the amount of carbon and fluorine remaining on the contact silicon surface layer. Figure 6 shows the XPS narrow scan spectra of fluorine [Fig. 6(a)] and carbon [Fig. 6(b)] measured on the exposed contact silicon surface of the patterned wafer. As references, XPS narrow scan data of a clean silicon wafer and a nonpatterned silicon wafer were included with the XPS narrow scan data of the patterned wafer after removal of the contact SiO_2 mold layer. Both of the reference wafers were also etched using HARC and cleaned with oxygen plasma. In Fig. 6, the nonpatterned silicon wafer shows higher fluorine and carbon peak intensities than the patterned silicon wafer. The clean silicon wafer does not show any fluorine peak intensity and shows a small but distinct carbon peak intensity, which may be due to the carbon contamination during exposure to the air. The lower carbon and fluorine peak intensities of the patterned silicon wafer appear to be related to the coexistence of a damaged contact bottom silicon area and an undamaged silicon area, which was covered by the contact SiO_2 mold layer during HARC etching. All of the silicon surface areas of the nonpatterned silicon wafer were damaged by HARC etching.

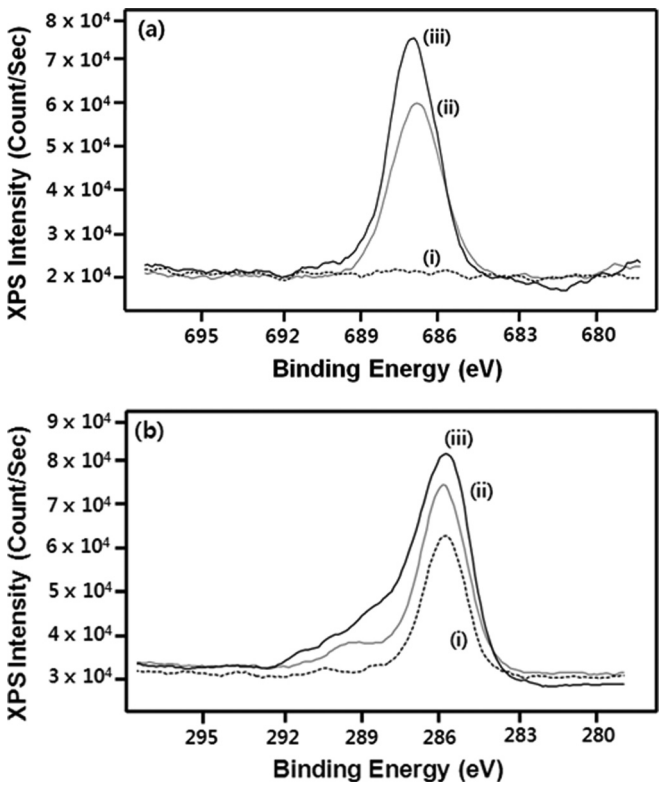

FIG. 6. XPS narrow scan spectra of (a) fluorine and (b) carbon after HARC etching and oxygen plasma etching from (i) the clean silicon wafer, (ii) the patterned wafer, and (iii) the nonpatterned wafer.

The depths of the carbon and fluorine penetration into the contact silicon surface were also investigated using a SIMS depth profile, and the results are shown in Fig. 7 for the nonpatterned and patterned wafers. The depths of penetration of fluorine and carbon for the nonpatterned silicon wafer can be estimated to be $\geq$15 nm. Again, we see that the peak intensities from the patterned wafer are about 25% less than those from the nonpatterned wafer, possibly due to the coexistence of an undamaged silicon area, covered by the contact SiO_2 mold layer, and the contact silicon area, damaged during the HARC etching. The depth of damage of the contact silicon layer by HARC etching can be estimated to be at least 15 nm, which indicates how much of the silicon layer in thickness that needs to be removed to achieve low contact resistivity.

By ALET with Cl_2 as described in Sec. II, the damaged silicon layer on the 30 nm HARC pattern was etched for various numbers of etch cycles. Figure 8 shows the 30 nm HARC profiles observed with SEM before ALET [Fig. 8(a)], after 10 cycles of ALET [Fig. 8(b)], and after 100 cycles of ALET [Fig. 8(c)]. As shown, an approximately 1–1.5 nm thick contact silicon layer was removed after 10 cycles of ALET and a ~15-nm-thick contact silicon layer after 100 cycles of ALET. The undamaged (100) silicon was, in fact, etched by ALET at about 0.136 nm/cycle, which gave an

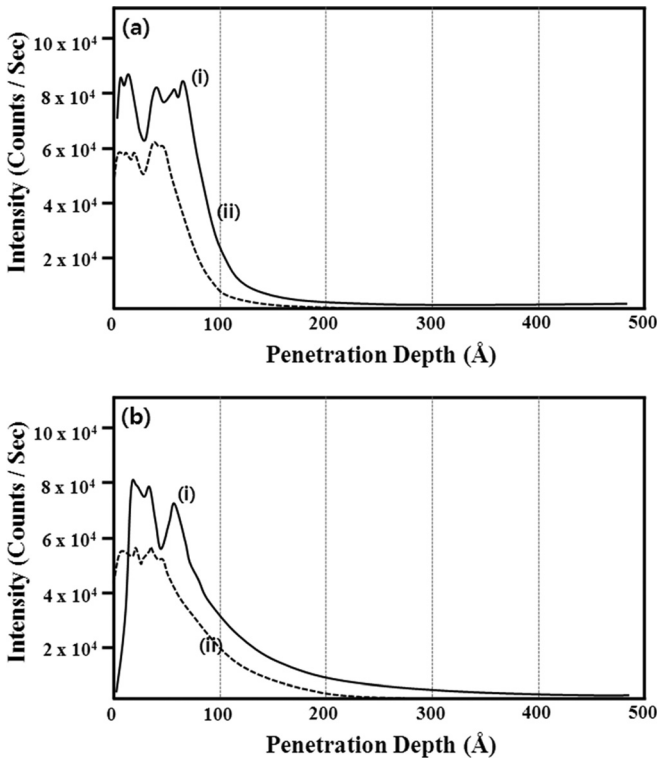

FIG. 7. SIMS depth profiles of (a) fluorine and (b) carbon after HARC etching and oxygen plasma etching from (i) the nonpatterned wafer and (ii) the patterned wafer.

etch distance of one atomic layer in the (100) direction. This resulted in the removal of ~13.56 nm of undamaged silicon after 100 cycles of ALET. However, we measured the etch rate for the damaged silicon to be higher, about 0.15 nm/cycle, which may have been due to the decreased binding energy of the damaged silicon. The measure of ~15 nm etched after 100 ALET cycles is consistent with previous investigations using nonpatterned blank silicon wafers.[12] In the case of contact SiO_2 mold profiles, as shown in Fig. 8, the contact top SiO_2 profile showed no significant degradation or pattern shape change (<5 nm) even after 100 cycles of ALET using Cl_2, probably due to the low energy (~25 eV) of the Ar beam used in the ALET processing. During ALET, the Cl_2 gas is adsorbed on both the contact silicon surface and the SiO_2 sidewall surface, but only the silicon chloride layer formed on the contact silicon surface was removed during the desorption step. There was no etching of the contact SiO_2 mold layer or removal of the silicon underlayer exposed after the removal of the chemisorbed silicon chloride layer during ALET. In fact, it is possible that no Cl_2 adsorption occurred on the SiO_2 surface during ALET because BCl_3, not Cl_2, is generally required for Cl_2 adsorption on oxides. Also, compared to an Ar ion beam, the neutral Ar beam penetrated better into the bottom of the deep contact through the deep and narrow SiO_2 contact hole without charging the contact SiO_2 surface and removed the chemisorbed silicon chlorides on the contact surface more easily. In addition, the ALET using low-energy Ar produced very little damage to the silicon surface and gave precise atomic-scale etch depth control. Therefore, it is believed that the contact silicon surface layer damaged by the 30 nm HARC etching can be effectively removed by ALET without degradation of the deep contact SiO_2 hole profile.

Atomic layer etching is similar to the atomic layer deposition process. However, it takes a long time to remove a 15-nm-thick silicon layer. Instead of using only ALET, therefore, we investigated the use of the combination of ALET and the conventional low-power CF_4 plasma treatment (ICP, 13.56 MH_z 1300 W_s, 13.56 MH_z 300 W_b, 5 mTorr, 20 s to remove ~15 nm). A previous study of nonpatterned silicon wafers[12] and the results shown in Fig. 1 demonstrate that the conventional low-power CF_4 plasma treatment causes secondary damage to the contact silicon, although the damage is not as significant as that produced by HARC etching. It is found that only 10 cycles of ALET is necessary to remove the secondary damage caused by the low-power CF_4 plasma treatment of the damaged contact silicon layer. Figure 9 shows the XPS narrow scan spectra of fluorine and carbon from the patterned silicon for the damaged state [after HARC etching and oxygen plasma processing, i.e., the same conditions as those of line ii plotted in Fig. 7(a)] and after 20 s of low-power CF_4 plasma treatment and 10 cycles of ALET. As a reference, XPS narrow scan data from a clean silicon wafer are also included. As shown in Fig. 9, after 20 s of CF_4 plasma treatment and 10 cycles of ALET, the peak intensities of carbon and fluorine of the

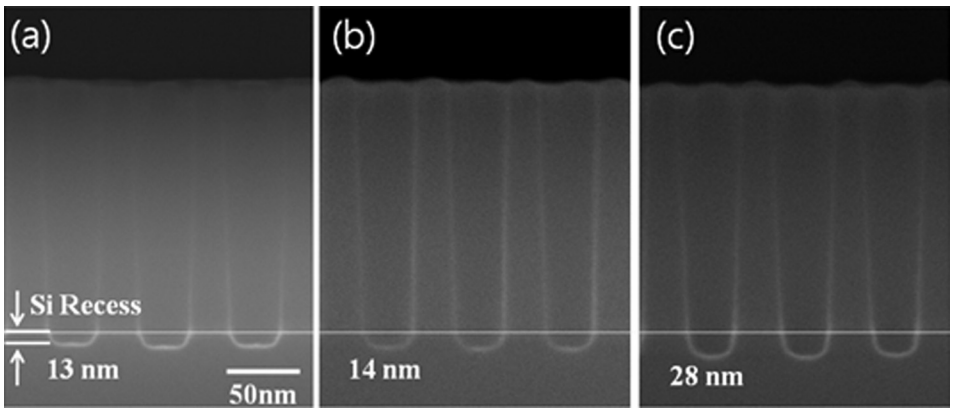

FIG. 8. SEM image of the 30 nm contact profile (a) in its initial status, (b) after 10 cycles of ALET, and (c) after 100 cycles of ALET.

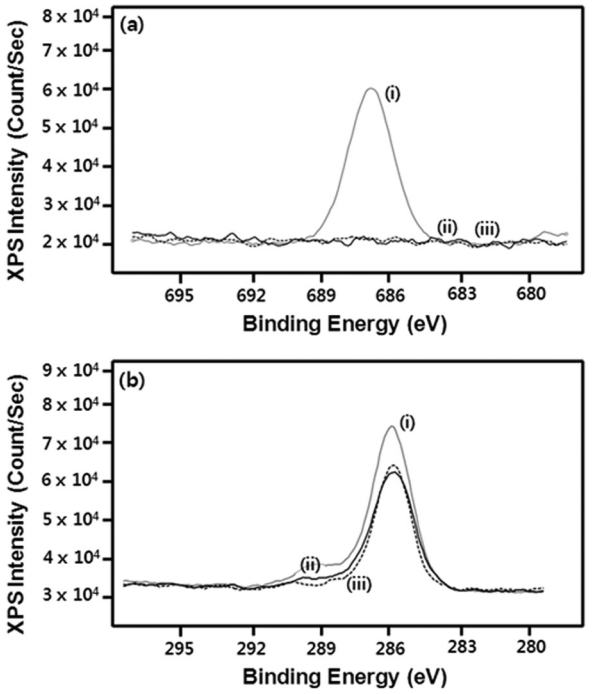

FIG. 9. XPS narrow scan spectra of (a) fluorine and (b) carbon from the patterned wafer (i) in its initial damaged state (HARC etching and oxygen plasma) and (ii) after the combined treatment using low-power CF_4 plasma for 20 s and 10 cycles of ALET. (iii) Also included is the spectrum from a clean silicon wafer surface for reference.

damaged silicon layer decreased to levels close to those of the clean silicon wafer. This demonstrates that our combined process is very effective at removing damage on a silicon surface created by HARC etching.

The effect that 10 cycles of ALET had on the contact resistance was estimated by exposing the contact silicon surfaces and measuring the sheet resistances of the contact silicon surfaces. Figure 10 shows the sheet resistances of the contact silicon surfaces for a clean silicon wafer after HARC etching and oxygen plasma processing, and after the subsequent removal of damaged contact silicon layers with two different treatments. The first treatment used only the low-power CF_4 plasma treatment for 20 s, and the second used the low power CF_4 plasma processing for 20 s and 10 cycles of ALET. As shown in Fig. 10, the silicon surface was damaged by high-energy reactive ions during the HARC etching, which increased the sheet resistance from 113 to 136 Ω/□ (~20%) compared to that of the clean silicon surface. When the damaged silicon contact surface layer was removed by the conventional low power CF_4 plasma treatment technique only, the sheet resistance decreased by about 9.5% to 123 Ω/□. However, the application of 10 cycles of ALET decreased the sheet resistance even further to 116 Ω/□ (~6.5%), which was close to that of the clean silicon surface. This indicates that the removal of the secondary damage due to the CF_4 plasma treatment using ALET can restore the contact resistance of the damaged silicon surface to that of a clean undamaged contact surface.

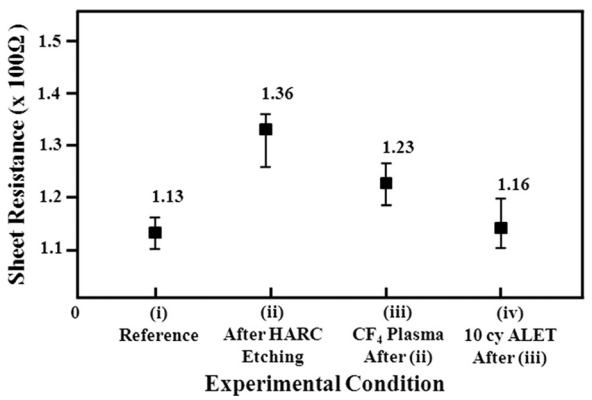

FIG. 10. Sheet resistances of the silicon surfaces of (i) a clean silicon reference wafer and (ii) a patterned wafer after the HARC etching and oxygen plasma treatment. Also, resistances were measured for the silicon surfaces presented (ii) after removal of the damaged layer using (iii) low-power CF_4 plasma treatment for 20 s and using (iv) the combined treatment using low-power CF_4 plasma for 20 s and 10 cycles of ALET. To measure the sheet resistance, the contact SiO_2 layer of the patterned silicon wafer is removed and the contact silicon surface is exposed.

IV. SUMMARY AND CONCLUSIONS

The damage on a 30 nm contact surface by HARC etching (8:1 aspect ratio) was removed by ALET, and the effects of ALET on the characteristics of the contact silicon were investigated. Similar to a nonpatterned silicon surface etched by the HARC etching process, a contact silicon surface patterned with a 30 nm ACL contact mask showed damage and contamination by carbon and fluorine, and the depth of penetration by carbon and fluorine into the silicon contact surface was at least 15 nm. This damaged silicon layer was removed using 100 cycles of ALET with Cl_2 without significant degradation and pattern shape change (<5 nm) of the contact top SiO_2 profile. Compared to the conventional low-power CF_4 plasma technique that causes secondary damage to the contact silicon surface, ALET does not cause any significant secondary damage to the contact surface and provides precise atomic-scale etch depth control. The secondary damage caused by the subsequent low-power CF_4 plasma treatment, used to remove the primary damage and contamination of the contact surface, was successfully removed by applying 10 cycles of ALET. This combined process overcame the problem of the slow etch rate of ALET. Once the secondary damage was removed, the resistance of the damaged HARC silicon surface was recovered to a level close to that of the clean silicon surface.

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