Solid-State Electronics 82 (2013) 82–85

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Letter

Improvement of metal gate/high-k dielectric CMOSFETs characteristics by atomic layer etching of high-k gate dielectric

K.S. Min [a,d,e], C. Park [e], C.Y. Kang [e], C.S. Park [e], B.J. Park [f], Y.W. Kim [b], B.H. Lee [c], Jack C. Lee [d], G. Bersuker [e], P. Kirsch [e], R. Jammy [e], G.Y. Yeom [a,*]

[a] Department of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, Gyeonggi-do 440-746, Republic of Korea
[b] Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Republic of Korea
[c] Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju 500-712, Republic of Korea
[d] Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, Austin, TX 78758, USA
[e] SEMATECH, Austin, TX 78741, USA
[f] Process Development Team, Semiconductor R&D Center, Samsung Electronics, San #16 Banwol-Dong, Hwasung-City, Gyeonggi-Do 445-701, Republic of Korea

A R T I C L E I N F O

Article history:
Received 31 July 2012
Received in revised form 15 November 2012
Accepted 21 November 2012
Available online 5 March 2013

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Plasma induced damage
Atomic layer etching
High-k dielectric
Complementary metal–oxide–semiconductor field effect transistors (CMOSFETs)

A B S T R A C T

Atomic layer etching (ALE) has been applied to the high-k dielectric patterning in complementary metal–oxide–semiconductor field effect transistors (CMOSFETs), and its electrical characteristics were compared with those etched by conventional etching such as wet etching (WE) or reactive ion etching (RIE). The CMOSFET etched by the ALE showed the improvement of the off-state leakage current (I_{off}), which was mainly attributed to the decreased perimeter component of the gate leakage current (I_G) particularly, at the low field region. The better electrical characteristics are due to the low trap density at the edge of gate oxides in the S/D region of CMOSFETs.

© 2013 Elsevier Ltd. All rights reserved.

1. Introduction

As the critical dimension (CD) of metal–oxide-semiconductor field effect transistor (MOSFET) is scaled down to tens of nanometer, the physical thickness of SiO_2 is intrinsically limited. Therefore, high-k dielectrics having higher physical thickness with the same equivalent oxide thickness (EOT) are investigated as an alternative to SiO_2. Among the numerous high-k dielectrics, hafnium oxide (HfO_2) has been presently integrated as the gate dielectric because it is stable and has a high dielectric constant (25), high thermal stability, and low interface states on the Si substrate [1].

For the high-k dielectric patterning, wet etching (WE) is used due to the thin thickness of the gate dielectric, the requirements of extremely high etch selectivity and low damage to the substrate. However, as the CD is scaled down to 32 nm node and below, plasma etching such as reactive ion etching (RIE) gradually becomes more important because it is difficult for WE to etch anisotropically and remove compounds such as $MeSi_xO_y$ formed at the interface between Me_xO_y and Si substrate. Even for plasma etching, it is important to etch with high etch selectivity over the substrate because the high-k dielectric must be etched from the source and drain regions without the silicon substrate recess. A previous study on HfO_2 etching showed that a high etch selectivity to the silicon substrate can be achieved using Ar/C_4F_8 gas compare to Ar/CF_4 gas in an inductively coupled plasma (ICP) [2]. High etch selectivity greater than 10 over the silicon could be also achieved using BCl_3/Cl_2 gas in an ICP [3]. However, plasma etching can introduce plasma induced damages (PIDs) and was found to degrade the electric characteristics and reliability including the positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI) in metal gate/high-k dielectric CMOSFETs [4–7].

There are two types of plasma induced damages (PIDs), which consist of plasma induced charging damage (PICD) and plasma induced edge damage (PIED) [8]. The former is originated from Fowler–Nordheim (FN) tunneling current through the gate oxide and the latter is caused by the direct HfO_2 plasma interaction and ion bombardment at the edge of gate oxide. Especially, as the gate oxide thickness is decreased to nanoscale, due to the increase of direct tunneling, PIED becomes more important in PID.

* Corresponding author. Tel.: +82 31 299 6560; fax: +82 31 299 6565.
E-mail address: gyyeom@skku.edu (G.Y. Yeom).

0038-1101/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2012.11.008

Previously, to solve the PIED, gate re-oxidation and plasma O_2 treatment of gate oxide, etc. have been investigated [9–12]. Gate re-oxidation has been successfully introduced to poly-Si/SiO_2 [9] but, due to the increase of equivalent oxide thickness (EOT) and a change in the effective work function, it cannot be easily applied to poly-Si/TiN/HfO_2/Si [10]. Plasma O_2 treatment was also demonstrated to encapsulate and passivate the gate edge leakage path for high-*k* dielectric structures, but the process reliability and uniformity is still in question [11,12].

Atomic layer etching (ALE) has been previously investigated to etch the material with a precise etch rate without introducing physical and chemical damage to the substrate [13–15]. ALE is a cyclic process similar to atomic layer deposition (ALD), and it is consisted of four steps: (1) adsorption of reactive gas, (2) evacuation of un-reacted reactive gas, (3) desorption of chemisorbed compound by energetic particle beam bombardment, and (4) evacuation. However, after the one cycle, one atomic layer is etched for ALE instead of the deposition of one atomic layer. The details of the ALE can be found elsewhere [16]. Previous results on the ALE of HfO_2 showed the constant etch depth of an atomic layer scale per cycle without changing the chemical composition of the etched HfO_2 surface [17].

In this article, to study the effect of ALE for high-*k* dielectric on the device properties systematically, ALE has been applied to the high-*k* dielectric in a metal gate/high-*k* dielectric CMOSFET, and its electrical characteristics were compared with those obtained after the etching of HfO_2 by WE and RIE.

2. Experimental

Metal gate/high-*k* dielectric CMOSFET devices with a gate width (*W*) of 10 μm and length (*L*) of 1 μm were fabricated using a standard complementary MOS process. The gate structure was consisted of chemical vapor deposition (CVD) deposited 1000 Å poly-Si, atomic layer deposition (ALD) deposited 100 Å TiN, 30 Å HfO_2, and 10 Å interfacial SiO_2 over Si substrate. Using a hard mask (HM), after metal gate etching by a conventional reactive ion etching (RIE), HfO_2 was etched with wet etching (WE) (the standard HfO_2 wet etching method is the etching of HfO_2 in a HF-based solution after the activation of HfO_2 with an Ar physical bombardment), using a HF based solution, or RIE (a BCl_3/Cl_2 inductively couple plasma with ~ -60 V of dc bias voltage), or ALE (experimental condition: 1st grid voltage: 60 V, Ar neutral beam irradiation dose: 2.11×10^{17} atoms/cm^{-2} (140 s), BCl_3 pressure: 0.33 mTorr, number of cycles: 30.

The etch depth was measured using a step profilemeter (Tencor Instrument, Alpha Step 500). The measured etch depth was divided by the total number of ALE cycles to have the etch rate per cycle. Capacitance–voltage (*C*–*V*) was measured on a metal–oxide-semiconductor capacitor (MOSCAP) structure with an area of 200 μm^2 using a precision LCR meter (Hewlett–Packard, 4284A) and current–voltage characteristics was measured on PMOSFETs and NMOSFETs using a semiconductor parameter analyzer (Hewlett–Packard, 4156B). X-ray photoelectron spectroscopy (XPS, Thermo VG, MultiLab 2000, Mg Kα source) was used to measure the stoichiometric modification of HfO_2 during the etching.

3. Results and discussion

Fig. 1 shows the characteristics of drain current (I_D)–gate voltage (V_G) for NMOSFET (the *W*/*L* of the device = 10/1 μm) after WE, RIE, and ALE. On-state current (I_{on}) at $V_G = V_{th} + 0.85$ V and $V_D = 1.2$ V for all devices was similar but, off-state current (I_{off}) at $V_G = 0$ V and $V_D = 1.2$ V for ALE was much lower than that for RIE while a slightly lower than that for WE, which was mainly attributed to the gate leakage current (I_G) generated by PIED.

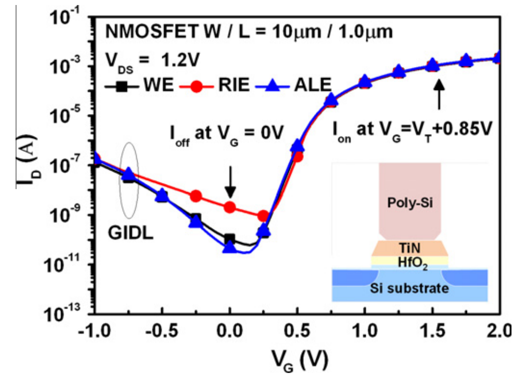

Fig. 1. The characteristics of drain current (ID)–gate voltage (VG) for NMOSFET (the *W*/*L* of the device = 10/1 μm) after WE, RIE, and ALE of HfO_2.

In fact, the I_{off} can be also affected by the etched gate edge profile of the high-*k* dielectric. The protruded high-*k* dielectric tend to decrease the I_{off} while the laterally recessed one tend to increase I_{off} due to the formation of the leakage path in the heterogeneous interface between the high-*k* dielectric and the capping nitride layer [18]. The origin of the change of I_{off} can be estimated by measuring gate-induced drain current (I_{GILD}), which is affected by the gate edge profile such as bird's beak. As shown in Fig. 1, the measured I_{GILD} values for WE, RIE, and ALE were similar to one another, respectively, suggesting that there is no significant change in the physical gate profile for WE, RIE, and ALE in a long channel device ($L = 1$ μm) investigated in this study. Therefore, the lowest I_{off} for ALE is believed to be caused by the decreased PIED instead of the gate profile during the high-*k* dielectric patterning.

Among the MOS parameters, gate leakage current (I_G) is the most sensitive to PIED because it changes the state of the gate oxide edge, which results in increasing the perimeter component rather than area one due to the formation of the additional I_G path at the edge of gate oxide near the source and drain (*S*/*D*) regions. Therefore, to classify I_G into the area and perimeter component, MOSCAP with shallow trench isolation (STI) and MOSFET with source/drain (*S*/*D*) structure were used. In the case of MOSCAP, due to the smaller gate oxide edge area compared to gate oxide area, I_G of MOSCAP tends to be more sensitive to the area than perimeter component of I_G. Therefore, the gate current density (J_G) of MOSCAPs with an area of 2×10^{-5} cm^2 was measured as a function of V_G after WE, RIE, and ALE as shown in Fig. 2a for PMOSCAP and NMOSCAP. No differences in J_G were found among them indicating that the area component of I_G was maintained. However, Fig. 2b shows the gate current density–gate voltage (J_G–V_G) measured for NMOSFET and PMOSFET (not shown here) with a $W/L = 10/1$ μm after WE, RIE, and ALE. The J_G–V_G could be divided into two distinctive regions. For the low V_G region, ALE exhibited a much lower J_G than RIE while showing a slightly lower I_G than WE. In contrast, at the high V_G region, the differences in J_G among them were decreased. It is known that, at the low V_G region, the gate tunneling current flows primarily to the edge of gate oxide near the *S*/*D* regions while the current mainly flows through the gate oxide at the high V_G region. Higher gate leakage current for the WE, RIE compared to ALE at the low V_G region could be originated from the perimeter component of I_G by the PIED rather than the area one, which resulted in increasing I_{off} as shown in Fig. 1.

To investigate the effect of PIED on gate oxide edge further, by using perimeter gate structure having the different length of gate dense line to increase the sidewall area of gate, the J_G of NMOSFET was measured at the low V_G region ($V_G = 0.5$ V), which is sensitive

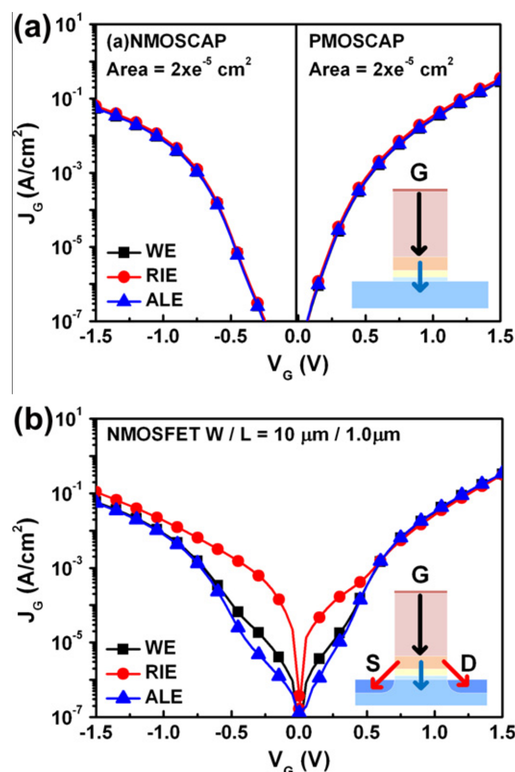

Fig. 2. Gate leakage current density-gate voltage (J_G–V_G) characteristics measured for (a) MOSCAP having shallow trench isolation (STI) with an area of 2×10^{-5} cm^2 and (b) MOSFET having source/drain (*S*/*D*) structure and with a *W*/*L* = 10/1 μm after WE, RIE, and ALE of HfO_2.

to the perimeter component of I_G by the PIED, after the etching by WE, RIE and ALE. As shown in the figure, the J_G was significantly increased for the denser perimeter structured gates after RIE while showing no significant change for the different length of gate dense line after ALE. Therefore, after the ALE of the high-*k* dielectric, the significant decrease of the PIED could be obtained.

In addition, to estimate the origin of the increased perimeter component of I_G by PIED, the surface composition of HfO_2 surface was measured by X-ray photoelectron spectroscopy (XPS). By using ALE compared to RIE, the stoichiometry of HfO_2 surface is maintained during the HfO_2 patterning. Fig. 4 shows the atomic percentages of Hf and O on the HfO_2 surface measured by XPS during the each ALE cycle. As comparison, the atomic percentage ratios of Hf/O on the HfO_2 surface before the etching (as-is) and after RIE were also included. As shown in the figure, during the

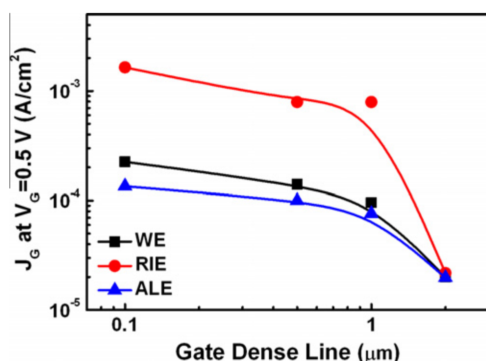

Fig. 3. Gate leakage current density characteristics measured for NMOSFET and PMOSFET (not shown here) of CMOSFET as a function of the different length of gate dense line for perimeter structured gates after WE, RIE, and ALE of HfO_2.

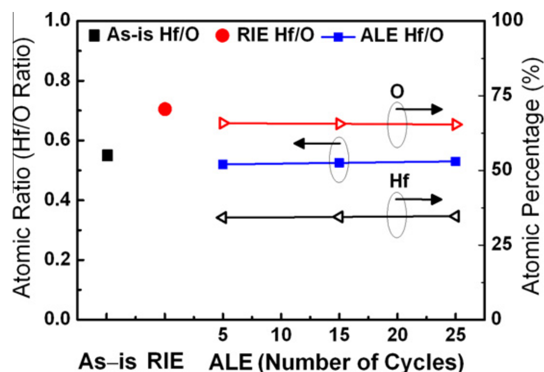

Fig. 4. Atomic percentages of Hf and O on the HfO_2 surface measured by X-ray photoelectron spectroscopy (XPS) during the each ALE cycle. As comparison, the atomic ratios of Hf/O on the HfO_2 surface before the etching (as-is) and after the etching by RIE were also included.

ALE, the atomic percentages of Hf and O were remaining similar during the ALE cycles because a monolayer was etched from the HfO_2 surface without the preferential removal of the component of HfO_2 such as Hf, or O per each cycle. Therefore, the atomic percentage ratio of Hf/O on the HfO_2 surface during ALE was also similar to that of as-is. However, in the case of RIE, the atomic percentage ratio of Hf/O was increased because it is preferentially etched more volatile component of HfO_2 such as BCl_xO_y due to the higher vapor pressure of BCl_xO_y compared with $HfCl_x$ formed as the etch products during the RIE. The change of surface composition during RIE will degrade the characteristics of HfO_2 by forming traps at the edge of the gate oxide near the *S*/*D* regions, which can be the additional gate leakage current path, therefore, the CMOSFETs etched by RIE showed noticeable PIED as observed in Figs. 1–3. However, by ALE, due to the no significant change of surface composition at the edge of gate oxide in addition to the exact silicon etch depth control, no significant PIED was observed.

4. Conclusions

In this study, ALE has been applied to the HfO_2 patterning after the TiN etching by RIE and its electrical characteristics of the CMOSFET were compared with those etched by WE or RIE. The CMOSFET etched by the ALE showed the improvement of I_{off}, which was mainly attributed to the decreased perimeter component of I_G particularly, at the low field region due to PIED. These results were related to the low edge damage of gate oxide during the ALE by maintaining the surface composition at the edge of gate oxide in addition to the exact control of silicon etch depth. It is believed that ALE is more beneficial to the high-*k* dielectric patterning of next generation CMOSFET, which can be applicable to low stand-by power (LSTP) devices.

Acknowledgments

This work was supported by the National Research Foundation of Korea Grant funded by the Korean Government (MEST) (NRF-2010-M1AWA001-2010-0026248) and was supported by MKE/KOTEF through the Human Resource Training Project for Strategic Technology.

References

[1] Robertson J. Eur Phys J Appl Phys 2004;28:265–91.
[2] Takahashi K, Ono K, Setsuhara Y. J Vac Sci Technol B 2005;23:6.
[3] Sha Lin, Chang Jane P. J Vac Sci Technol A 2003;21:1915.

[4] Tzeng PJ, Chang YY, Chang-Liao KS. IEEE Electron Device Lett 2001;22:11.
[5] Hussain MM, Song SC, Barnett J, Kang CY, Gebara G, Sassman B, et al. IEEE Electron Device Lett 2006;27:12.
[6] Min KS, Kang CY, Yoo OS, Park BJ, Kin SW, Young CD, et al. Proc Int Rel Phys Symp 2008:723.
[7] Wenga WT, Lee YJ, Lin HC, Huang TY. Solid-State Electron 2010;54:368–77.
[8] Chen SJ, Chung SSS, Lin HC. Jpn J Appl Phys 2002;41.
[9] Broiek T, Prabhakar V, Werking J, Chan YD, Viswanathan CR. Proc Int Rel Phys Symp 2002;41.
[10] Park CS, Song SC, Burham C, Park HB, Niimi H, Ju BS, et al. in Proc. Extended Abstract Int. Conf. Solid State Dev Mater 2007; 14–15.
[11] Ju BS, Song SC, Sassman CB, Kang CY, Lee BH, Jammy R. Technol Dig – Int Electron Devices Meet 2006.
[12] Ju BS, Song SC, Lee TH, Sassman B, Kang CY, Lee BH, et al. Proc Int Rel Phys Symp 2007:672.
[13] Matsuura T, Murota J, Sawada Y. Appl Phys Lett 1993;63:2803.
[14] Kim BJ, Chung SH, Cho SM. Appl Surf Sci 2002;187:124.
[15] Athavale SD, Economou DJ. J Vac Sci Technol B 1996;14:3702.
[16] Park SD, Oh CK, Bae JW, Yeom GY, Kim TW, Song JI, et al. Appl Phys Lett 2006;89:043109.
[17] Park SD, Oh CK, Lee DH, Yeom GY. Electrochem Solid-State Lett 2005;8:C117.
[18] Kang CY, Choi Rino, Song SC, Lee BH. Appl Phys Lett 2007;90:183501.