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Improvement of surface roughness in silicon-on-insulator wafer fabrication using a neutral beam etching

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Abstract

Silicon-on-insulator (SOI) wafers were etched by an energetic chlorine neutral beam obtained by the low-angle forward reflection of an ion beam, and the surface roughness of the etched wafers was compared with that of the SOI wafers etched by an energetic chlorine ion beam. When the ion beam was used to etch the silicon layer of the SOI wafers, the surface roughness was not significantly changed even though the use of higher ion bombardment energy slightly decreased the surface roughness of the SOI wafer. However, when the chlorine neutral beam was used instead of the chlorine ion beam having a similar beam energy, the surface roughness of the SOI wafer was significantly improved compared with that etched by the chlorine ion beam. By etching about 150 nm silicon from the SOI wafer having a 300 nm-thick top silicon layer with the chlorine neutral beam at the energy of 500 eV, the rms surface roughness of 1.5 Å could be obtained with the etch rate of about 750 Å min^{-1}.

1. Introduction

For next generation silicon substrates applied to nano-scale semiconductor devices, silicon-on-insulator (SOI) wafers are known to be one of the outstanding candidates because of advantages such as high speed, high packing density, immunity from latch-up, low power dissipation and high resistance to ionizing radiation. One of the most advanced methods in the fabrication of SOI wafers is the smart-cut method. Here, a few hundred-nanometre-thick top silicon layer is detached from the silicon wafer to the oxide wafer for the SOI by forming many micro-voids in the silicon wafer through the implantation of hydrogen in it [1–3].

After the formation of a SOI wafer by the smart-cut method, the top silicon layer of the SOI wafer is etched down to a certain thickness for device fabrication and the surface roughness is also removed during etching. In particular, the surface roughness of the silicon top layer of the split SOI wafer is very important because it can change the physical and chemical properties of the top silicon layer of the SOI wafer. Compared with bulk silicon, as the thickness of the top silicon layer of the SOI wafer is thinner, the effective carrier mobility is more affected by the surface roughness of the silicon layer through the increased scattering of carriers with the surface and interfaces [4–6].

Many approaches have been attempted to reduce the surface roughness of the top silicon wafer by chemical mechanical polishing, high temperature annealing, wet etching, etc, but these methods are known to have some problems such as long processing time and reliability of exact thickness control [7–9]. One of the methods that can obtain more reliable thickness control is dry etching; however, dry etching such as plasma etching and reactive ion etching does not significantly improve the surface roughness during the etching of the top silicon layer possibly due to the charging of the top silicon layer of the SOI wafer during the etching. If the top silicon layer can be thinned down with a smooth silicon surface by dry etching, improved device properties can be expected for the nano-scale device fabrication [10].

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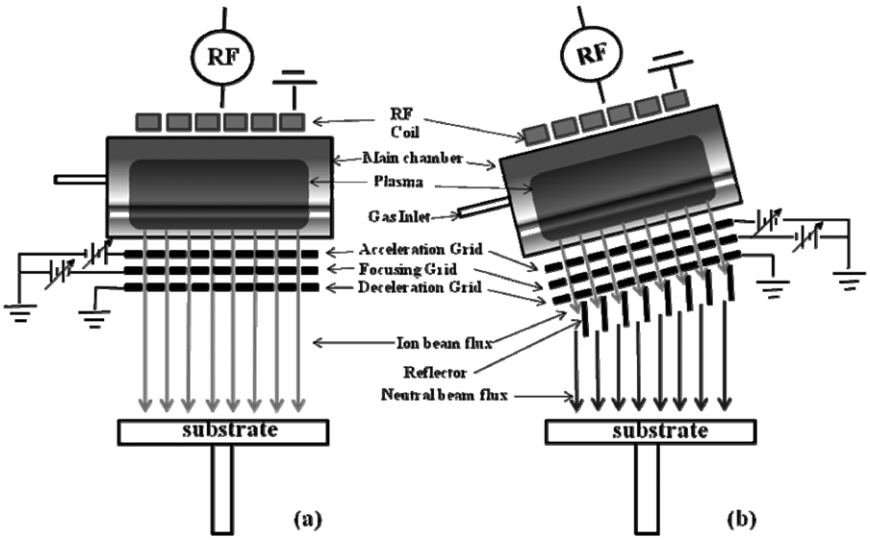

Figure 1. Schematic diagram of (*a*) the ICP-type ion beam etching system and (*b*) the low-angle forward-reflected neutral beam etching system used in the experiment.

Neutral beam etching has been investigated by many researchers to etch nano-scale semiconductor materials without charge-related damages to the devices [11–13]. In this study, one of the neutral beam etching techniques called 'low-angle forward-reflected neutral beam etching' has been used to control the thickness of the top silicon layer and the surface roughness etched by neutral beam etching was compared with that etched by an ion beam to study the effect of neutral beam on the control of the surface roughness of the top silicon layer of the SOI wafer.

2. Experimental

Figure 1 shows (*a*) the ion beam source and (*b*) the neutral beam source used in this experiment to etch the top silicon layer of the SOI wafer. The ion beam source was an inductively coupled plasma (ICP)-type ion gun composed of an ICP source for the plasma generation and three grids for the ion acceleration. For the neutral beam source, parallel low-angle reflectors were located in front of the three grids as shown in figure 1(*b*) to reflect the ions extracted from the ion gun and to form a neutral beam by the reflection on the parallel reflectors. 300 W, 13.56 MHz rf power was applied to the ICP source and, to extract the ions from the plasma source, positive voltages were applied to the first grid close to the plasma source to vary the beam energy, and a negative voltage was applied to the second grid to focus the ion beam and to control the flux of the ions extracted from the source, and the third grid was grounded. For the neutral beam, the ion beam extracted from the ion gun was reflected on the grounded parallel-plate-type reflectors which have a 5° slope to the ion beam direction for the formation of a parallel neutral beam. The reflectors and grids used in the experimental systems were fabricated with graphite to minimize the possible contamination on the substrate. The neutralization efficiency of the neutral beam obtained after the reflection of the ion beam on the reflector was higher than 99% [14]. Cl_2 was used as the etch gas, and its gas flow rate was varied from 5 to 30 sccm. The base pressure of the processing chamber was lower than 4×10^{-7} Torr, and when 30 sccm Cl_2 was used, the processing chamber pressure was increased to 5×10^{-4} Torr. Grid voltages of 100–500 V were applied to the first grid of the source to control the beam energy while −700 V was applied to the second grid.

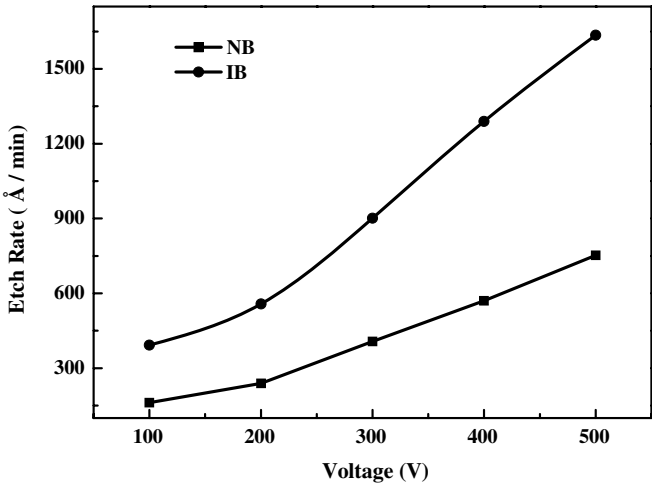

Figure 2. Etch rates of the top silicon layer of the SOI wafer for the neutral beam (NB) etching and the ion beam (IB) etching measured as a function of the first grid voltage (∼particle beam energy) at 15 sccm of Cl_2.

For the SOI wafer, as-split SOI wafers having a top silicon layer thickness of about 300 nm was used as the sample. In addition, SOI wafers annealed at 1200 °C in N_2 for 12 h to remove hydrogen defects in the silicon layer were also used. The thickness of the top silicon layer of the SOI wafer was decreased to about 270 nm after annealing. The surface roughness before etching and after etching was measured using an atomic force microscopy (AFM, Park Systems XE100) and the etch rate was measured by measuring the etch depth using a step profilometer (Tencor Alpha-Step 500).

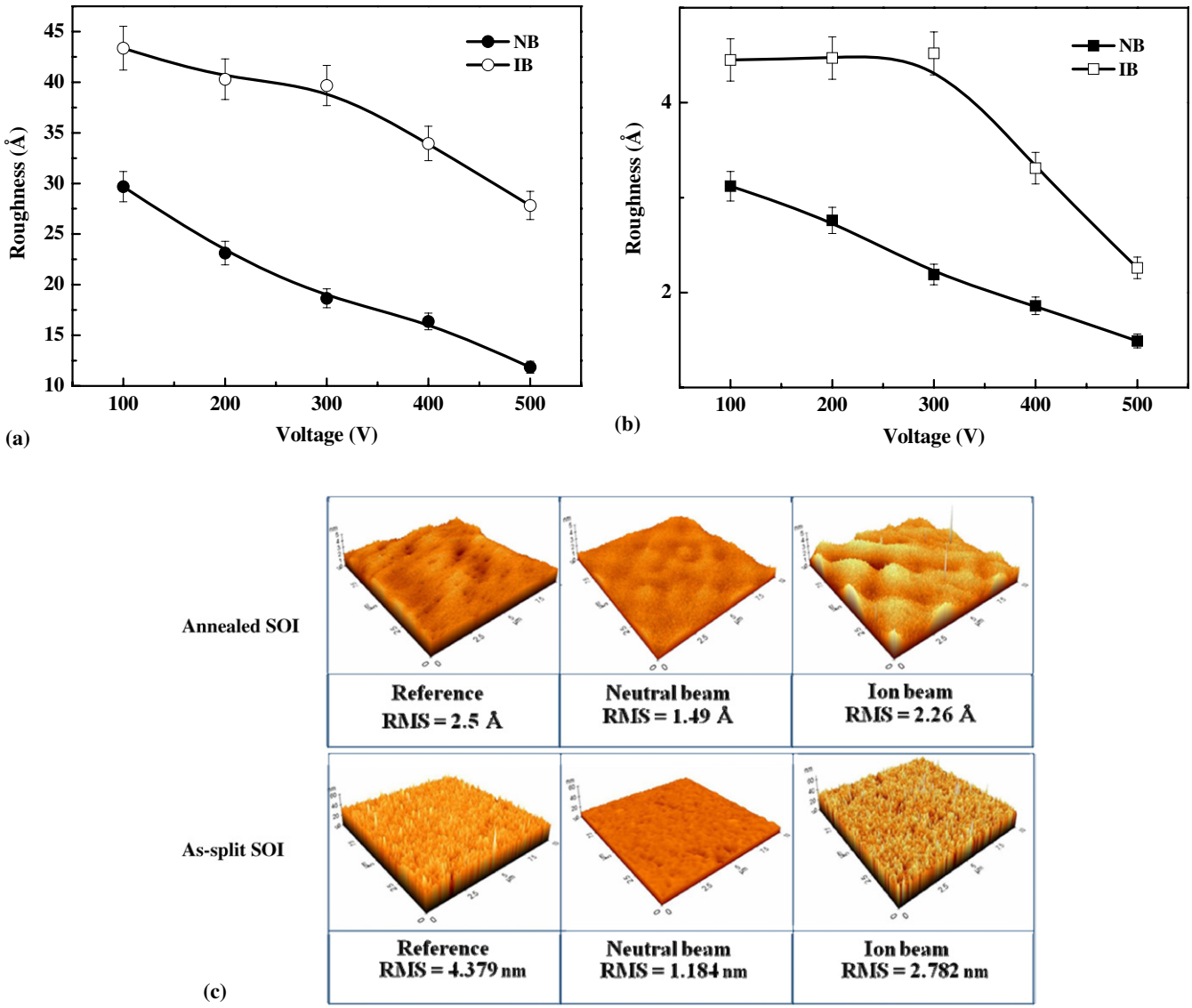

Figure 3. The rms surface roughness measured on the 100 nm-thick remaining top silicon after the etching of (*a*) the as-split annealed SOI wafer (before the etching, the rms roughness of 300 nm-thick top silicon layer was 43.79 Å) and (*b*) the annealed SOI wafer (before the etching, the rms roughness of the 270 nm-thick top silicon layer was 2.5 Å). (*c*) shows the AFM images of SOI wafer surfaces before/after etching with the first grid voltage of 500 V.

(This figure is in colour only in the electronic version)

3. Results and discussion

The top silicon layer of the SOI wafer (both as-split and annealed) was etched using a neutral beam and an ion beam by varying the Cl_2 gas flow rate and the first grid voltage (for the change of the beam energy) while maintaining the second grid voltage at −700 V. At first, while keeping the first grid voltage constant, the Cl_2 gas flow rate was varied from 5 to 30 sccm, and the silicon etch rate was the highest at 15 sccm for both the neutral beam etching and the ion beam etching. The highest silicon etch rates obtained at 15 sccm appear to be related to the highest plasma density in the ICP source at 15 sccm. Therefore, while keeping the Cl_2 gas flow rate at 15 sccm, the etch rate was measured as a function of the first grid voltage, and the results are shown in figure 2. The silicon etch rate was not significantly different for both as-split silicon and annealed silicon. As shown in the figure, the silicon etch rate increased with the increase in the first grid voltage for both neutral beam etching and ion beam etching due to the increase in beam impingement energy to the silicon surface. As the grid voltage was increased from 100 to 500 V, for the neutral beam etching the etch rate increased almost linearly from 160 to 750 Å min^{-1}, and for the ion beam etching also the etch rate increased almost linearly from 390 to 1640 Å min^{-1}. Therefore, at the same first grid voltage, the ion beam etching showed about two times higher etch rate compared with the neutral beam etching. Previous experiments showed that the neutral beam energy and flux decreased slightly after the reflection of the beam on the reflector due to the energy transfer to the reflector and the beam scattering during the reflection even though the grid voltages were maintained the same for both the ion beam and the neutral beam [14]. Therefore, the

lower etch rate obtained for the neutral beam etching at the same first grid voltage (incident beam energy) is related to the decreased beam energy and flux after the reflection on the reflector.

For each etching condition, the remaining top silicon thickness of the SOI wafer was etched down to 100 nm for high performance device fabrication and the surface roughness was measured using AFM. The results are shown in figure 3(*a*) for the surface roughness of the top silicon etched using the as-split SOI wafer and in figure 3(*b*) for the roughness of the top silicon etched using the annealed SOI wafer. Figure 3(*c*) shows the AFM images of the SOI wafer surfaces for figures 3(*a*) and (*b*) before/after etching at the first grid voltage of +500 V. The surface roughness was measured as a function of the first grid voltage for the neutral beam and for the ion beam. When the surface roughness of the top silicon of the SOI wafer was measured for the as-split SOI wafer and for the annealed SOI wafer before etching by the neutral beam and the ion beam, an rms surface roughness of about 43.8 Å was measured for the as-split SOI wafer while about 2.5 Å was observed for the annealed SOI wafer. The significantly lower surface roughness obtained for the SOI wafer annealed at 1200 °C in N_2 for 12 h is related to the rearrangement of the silicon lattice by the removal of the micro-voids and hydrogen in the silicon layer of the SOI wafer. It is known that the Si–H bonding is broken in the temperature range 200–500 °C and hydrogen in the silicon layer diffuses out at temperatures higher than 500 °C, which results in a decrease in the surface roughness after annealing [15, 16].

As shown in figure 3, when the silicon was etched with the first grid voltage lower than 300 V, especially for the ion beam etching, the surface roughness increased a little after the etching. However, as the first grid voltage was increased, the surface roughness generally decreased with increasing first grid voltage, and at the same first grid voltage the surface roughness etched using the energetic chlorine neutral beam was much lower compared with that etched using the energetic chlorine ion beam. At about 500 V of the first grid voltage, the rms surface roughness about 27.8 Å after the ion beam etching and about 11.8 Å after the neutral beam etching could be observed for the as-split SOI wafers. For the annealed SOI wafers, at the same first grid voltage, the rms surface roughness about 2.3 Å after the ion beam etching and about 1.5 Å after the neutral beam etching could be observed. The slight increase in surface roughness observed after the etching of the SOI wafer at lower first grid voltages appears to be related to the defects and residues remaining on the silicon surface before the etching, which causes micromasking during the etching. However, the decrease in surface roughness observed after the etching at the higher first grid voltages appears to be related to the decreased etch selectivity over micromasking materials such as defects and residues at the high bombardment energy. In general, if there is no micromasking and if there are no charge-related issues, the surface roughness decreased with increasing etch depth. Figure 4 shows the well-known sputter etch yield versus incident angle of the bombarding particle [17, 18]. As shown in figure 4, the sputter etch yield increased with increasing angle of incidence (θ) as a function of sec θ, showing a maximum sputter etch yield at an incident angle <90° and finally decreased to zero at an incident angle of 90°. Therefore, a flat surface which makes a 0° incident angle is etched slower than a rough surface which makes the angle between 0° and 90°, and the surface roughness decreased with increasing etch depth as shown in figure 3 for higher bombardment energies.

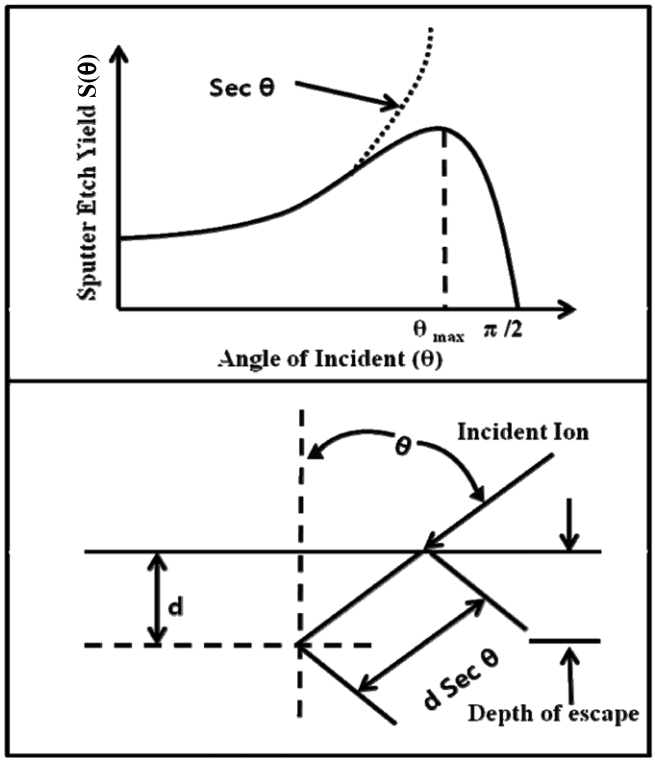

Figure 4. Sputter etch yield versus incident angle of the bombarding particle.

When a chlorine ion beam is used for the etching of the SOI wafer, the top silicon layer is charged positively due to the chlorine ion bombardment and, as shown in the top figure of figure 5(*a*), the charge is concentrated on the facet of the rough surface and a high electric field is formed on it. Due to the high electric field, the chlorine ions incident on the top silicon layer of the SOI wafer tend to bend away from the facet of the rough surface, especially for the lower ion bombardment energies, and a rough surface is maintained after the etching of the surface, as shown in the bottom figure of figure 5(*a*) even though there is no micromasking on the SOI wafer surface. However, in the case of chlorine neutral beam etching, because the bombarding particles do not contain the charge, the SOI wafer is not charged during the etching, as shown in the top figure of figure 5(*b*), therefore, the rough facet surface is etched faster than the flat surface as shown in the bottom figure of figure 5(*b*) by the mechanism shown in figure 4. Therefore, after the etching by the chlorine neutral beam, a much smoother surface compared with the surface etched by the ion beam could be obtained.

4. Conclusions

The top silicon layer of an SOI wafer of about 300 nm (~270 nm for the annealed silicon) was etched by an energetic

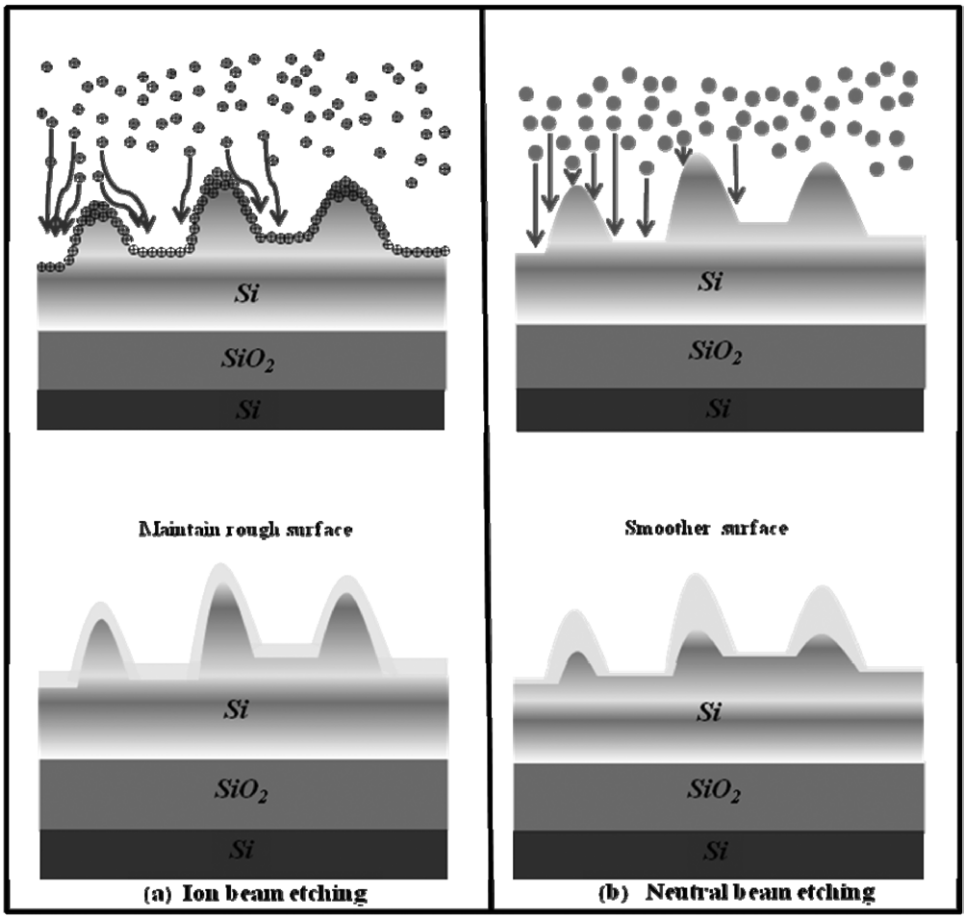

Figure 5. Top silicon etch mechanism of the SOI wafer by (*a*) an ion beam and (*b*) a neutral beam.

chlorine neutral beam and the surface roughness of the remaining 100 nm-thick silicon surface was compared with that etched by an energetic chlorine ion beam under the same etch process conditions. When the top silicon layer was etched by a chlorine-based neutral beam at 15 sccm of Cl_2, the etch rate increased with the increase in neutral beam energy showing about 750 Å min^{-1} at 500 V of the first grid voltage (∼neutral beam energy); however, the etch rate was about half of that etched by the chlorine-based ion beam under similar operation conditions of the ion source. When the surface roughness was compared after the etching of the SOI wafer down to the remaining 100 nm-thick top silicon layer, the surface roughness of the SOI wafer etched by the neutral beam was much lower compared with that etched by the ion beam under similar conditions. At about 500 V of the first grid voltage, for the annealed SOI wafer, the rms surface roughness decreased from 2.5 to about 2.3 Å after the ion beam etching and to about 1.5 Å after the neutral beam etching. The improvement of the surface roughness after the etching by a neutral beam was related to the well-known relationship between the sputter etch yield and the incident angle of the bombarding particle, where a rough facet surface is etched faster than the flat surface. However, in the case of ion beam etching, due to the charging of the facet of the rough surface, the rough facet surface was not significantly etched faster than the flat surface and no significant improvement of the surface roughness could be observed. Therefore, it is believed that a SOI wafer with a thin and smooth silicon top layer which can be applicable to nano-scale device processing could be obtained by applying neutral beam etching.

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