Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ p-HEMTs

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***Abstract*—The characteristics of 0.15-μm InAlAs/InGaAs pseudomorphic high-electron mobility transistors (p-HEMTs) that were fabricated using the Ne-based atomic layer etching (ALET) technology and the Ar-based conventional reactive ion etching (RIE) technology were investigated. As compared with the RIE, the ALET used a much lower plasma energy and thus produced much lower plasma-induced damages to the surface and bulk of the $In_{0.52}Al_{0.48}As$ barrier and showed a much higher etch selectivity ($\sim$70) of the InP spacer against the $In_{0.52}Al_{0.48}As$ barrier. The 0.15-μm InAlAs/InGaAs p-HEMTs that were fabricated using the ALET exhibited improved $G_{M,\max}$ (1.38 S/mm), $I_{\rm ON}/I_{\rm OFF}(1.18 \times 10^4)$, drain-induced barrier lowering (80 mV/V), threshold voltage uniformity ($V_{\rm th,avg} = -190$ mV and $\sigma = 15$ mV), and f_T (233 GHz), mainly due to the extremely low plasma-induced damage in the Schottky gate area.**

***Index Terms*—Atomic layer etching (ALET), drain-induced barrier lowering (DIBL), $I_{\rm ON}/I_{\rm OFF}$ ratio, pseudomorphic high-electron mobility transistor (p-HEMT), subthreshold slope.**

I. Introduction

INP-BASED InGaAs/InAlAs high-electron mobility transistors (HEMTs) have shown a remarkable performance improvement over the past two decades due to the excellent electron transport properties originating from the small effective electron mass in the channel and large conduction band discontinuity (ΔE_C). For fabrication of high-performance InGaAs/InAlAs HEMTs, an InP etch-stop layer is typically used for the improvement in overall performance and uniformity [1], [2]. However, the InP etch-stop layer is known to have a low Schottky barrier height ($\Phi_B = \sim$0.3 eV), leading to an excessive gate leakage current and, thus, a low breakdown behavior [3], [4]. To resolve such problems, Suemitsu *et al.* proposed a two-step recess technology, in which a selective wet etching was used to isotropically remove the heavily doped InGaAs/InAlAs cap layer, followed by an Ar-based plasma etching to anisotropically remove the InP etch-stop layer [1]. The use of the Ar-based plasma etching considerably improved the breakdown voltage since the Schottky gate was formed on the exposed $In_{0.52}Al_{0.48}As$ barrier. However, the Ar-based plasma etching has a finite etch selectivity ($\leq$ 20) of InP against $In_{0.52}Al_{0.48}As$ [5]. More seriously, the Ar-based plasma etching usually uses highly energetic reactive ions to achieve a vertical etch profile and, thus, tends to produce plasma-induced damages at the surface and in the bulk of the $In_{0.52}Al_{0.48}As$ barrier layer, resulting in increased surface roughness and change of surface stoichiometry [6]–[9]. This damage eventually leads to the degradation of Schottky gate and overall device characteristics. Recently, Park *et al.* have successfully demonstrated a Ne-based atomic layer etching (ALET) to selectively remove a molecular beam epitaxy (MBE)-grown InP layer against an $In_{0.52}Al_{0.48}As$ layer [10]. The ALET, which used a low plasma energy and removed one monolayer of InP per unit etch cycle (corresponding to the InP etch rate of 1.47 Å/cycle), had an extremely high etch selectivity of 70 and exhibited smooth $In_{0.52}Al_{0.48}As$ surface and insignificant change of stoichiometry. Schottky diodes that were fabricated by the ALET thus showed better characteristics in terms of reverse leakage current, Schottky barrier height Φ_B, and ideality factor η [10]–[12]. In this letter, we have compared the characteristics of 0.15-μm InAlAs/InGaAs pseudomorphic HEMTs (p-HEMTs) that were fabricated using the ALET and RIE technologies.

II. Experiments

The InAlAs/InGaAs p-HEMT structure was grown by an MBE on a semi-insulating InP substrate and consisted of a 5000-Å $In_{0.52}Al_{0.48}As$ buffer, a 130-Å $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel, a 30-Å $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping (5×10^{12} cm^{-2}), an 80-Å $In_{0.52}Al_{0.48}As$ barrier, a 60-Å InP etch stop, and a 350-Å heavily doped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ multilayer cap. The fabrication process for the 0.15-μm p-HEMTs began with a mesa isolation down to the InAlAs buffer layer by a wet chemical etching. After source and drain ohmic metallization (Ni/Ge/Au = 100/450/1500 Å), a subsequent rapid thermal annealing at 275 °C was performed under N_2 ambient. Then, pad patterns for ground–signal–ground RF probes were defined by liftoff of

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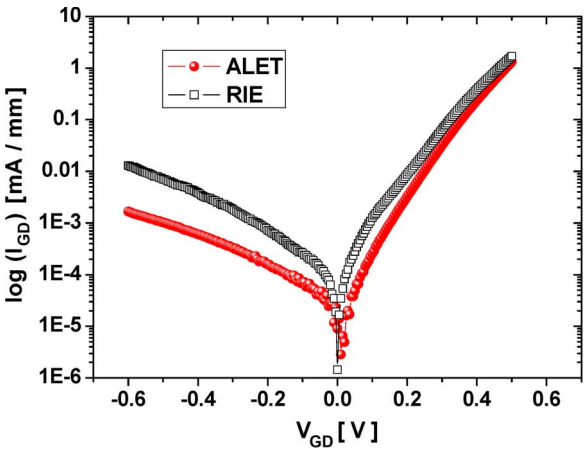

Fig. 1. Gate Schottky diode characteristics of the 0.15-μm InAlAs/InGaAs p-HEMTs with a gate width of 20 μm that were barricaded using the Ne-based ALET technology and the conventional Ar-based RIE technology.

Ti(200 Å)/Au (3000 Å). After coating the trilayer e-beam resists (PMMA/P(MMA-MAA)/PMMA), a double e-beam exposure method was used to define a 0.15-μm T-gate. After the InGaAs/n-InAlAs multilayer cap was isotropically removed by a citric acid-based wet solution, the Ne-based ALET technology was applied to remove the InP etch-stop layer. The ALET process consisted of four sequential steps: 1) introduction of Cl_2 gas into the etching chamber for 20 s so that the chlorine can be adsorbed on the surface of InP (adsorption step); 2) evacuation of the Cl_2 gas from the chamber; 3) Ne neutral beam irradiation to the Cl_2 adsorbed InP surface for desorption of InP chlorides (desorption step); and 4) evacuation of the InP chlorides from the chamber. Detailed process conditions can be found in [10]. For comparison, the conventional Ar-based plasma etching was also performed to etch the InP layer with a process pressure of 10 mtorr, an Ar flow of 50 sccm, and an RF power of 7 W in an Oxford Plasma Lab-80 RIE chamber. The etch rate of InP was 1.47 Å/cycle for the ALET and 4 Å/min for the RIE. Finally, gate metallization was done using Ti/Pt/Au (200/200/3000 Å).

III. Results and Discussion

Fig. 1 shows the Schottky diode characteristics of the 0.15-μm p-HEMTs with a gate width of 20 μm that were fabricated by the ALET and RIE. The ALET devices show better ideality factor and Schottky barrier height ($\eta = 1.61$, $\Phi_B = 0.44$ eV) than those ($\eta = 1.92$, $\Phi_B = 0.39$ eV) of the RIE devices. Here, the Φ_B was extracted using the standard current–voltage (I–V) technique [13]. The higher Φ_B and lower η of the ALET devices are attributed to the lower physical damage of the ALET to the underlying $In_{0.52}Al_{0.48}As$ barrier [11]. Using angular-resolved X-ray photoelectron spectroscopy, no significant change of the surface composition of the $In_{0.52}Al_{0.48}As$ barrier layer was observed after the ALET, whereas a significant decrease in the ratios of Al/In and As/InAl was observed in the case of the RIE [11]. Fig. 2 shows the transconductance G_M, output current $I_{\rm DS}$, and I–V characteristics of both devices. The ALET devices showed a higher $G_{M,\max}$ (1.38 S/mm) than that (1.1 S/mm) of the RIE

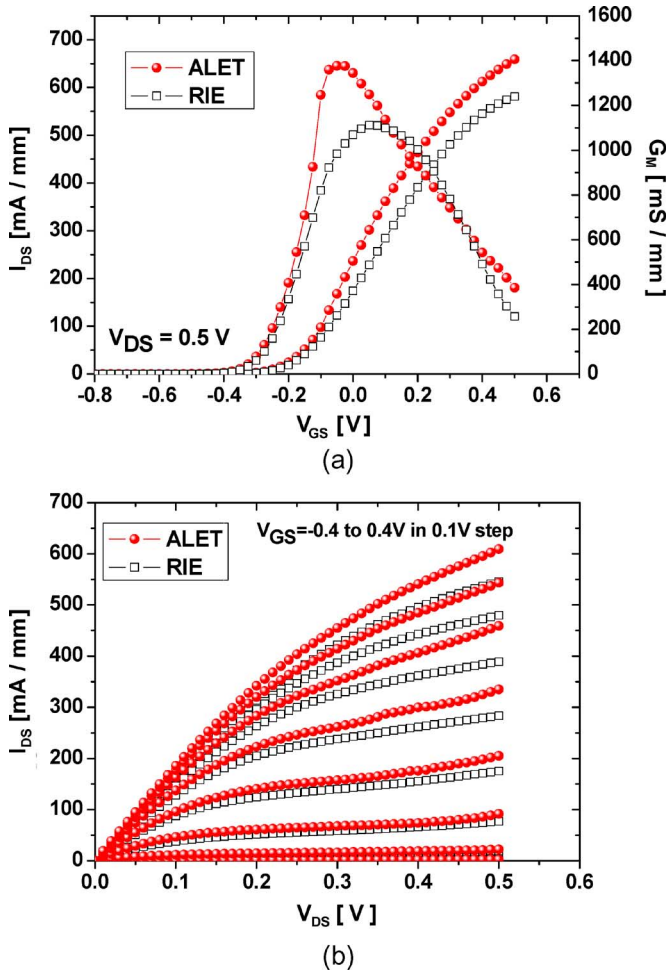

Fig. 2. (a) Drain current and dc transconductance as a function of the gate–source voltage. (b) Typical $I_{\rm DS}$–$V_{\rm DS}$ characteristics of the 0.15-μm InAlAs/InGaAs p-HEMTs.

devices at $V_{\rm DS} = 0.5$ V. The ALET device also showed a higher output conductance at the same drain current than the RIE device. Since the output conductance of a submicrometer p-HEMT is closely related to the gate hole current component, measurements of the gate leakage characteristics were carried out to extract the gate hole current components. The extracted peak gate hole current $I_{g,\rm hole}$ following the procedure described in [14] was 12 μA/mm for the ALET device and 5.5 μA/mm for the RIE device. The smaller gate hole current of the RIE device is presumably attributed to the reduced peak electric field between the gate and drain of the RIE device, due to the decreased channel mobility and thus the increased channel resistance caused by the plasma etching damage. Fig. 3 shows the subthreshold characteristics for both devices measured at $V_{\rm DS} = 0.05$ and 0.5 V. The $I_{\rm ON}/I_{\rm OFF}$ ratio and drain-induced barrier lowering (DIBL) of the ALET devices (1.18×10^4 and 80 mV/V) are better than those of the RIE devices (3.6×10^3 and 133 mV/V). Improvements of the $I_{\rm ON}/I_{\rm OFF}$ ratio and DIBL are associated with the improved Schottky gate characteristics of the ALET devices, as shown in Fig. 1. The ALET devices also showed an improved uniformity of the threshold voltage ($V_{\rm th,avg} = -190$ mV and $\sigma = 15$ mV), as compared with that ($V_{\rm th,avg} = -175$ mV and $\sigma = 22$ mV) of the RIE

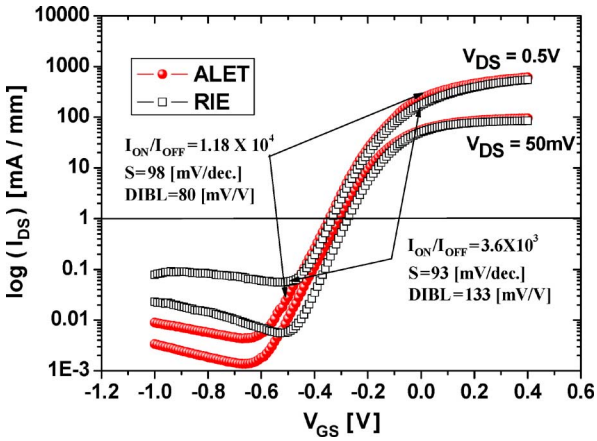

Fig. 3. Dependence of the drain current on the gate–source voltage of the p-HEMTs biased at $V_{\rm DS} = 0.05$ and 0.5 V. $I_{\rm ON}$ is defined as the $I_{\rm DS}$ at $V_{\rm GS} = V_{\rm th} + 2/3\ V_{\rm DS}$, and $I_{\rm OFF}$ is defined as the $I_{\rm DS}$ at $V_{\rm GS} = V_{\rm th} - 1/2\ V_{\rm DS}$. The subthreshold slope S is defined as the change of the gate–source voltage when the $I_{\rm DS}$ changes by an order of magnitude in the subthreshold region. DIBL is defined as $\Delta V_{\rm th}/\Delta V_{\rm DS}$ [15].

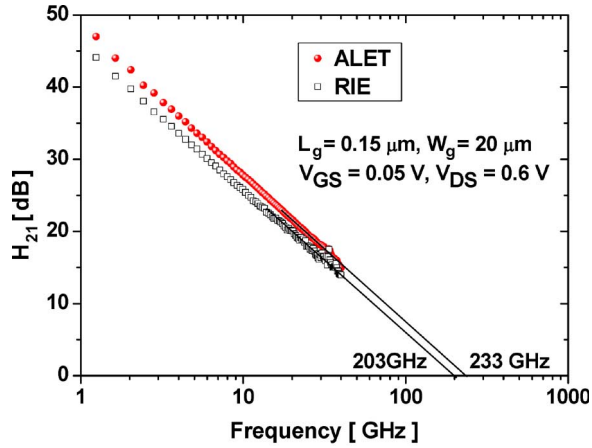

Fig. 4. Microwave characteristics of the 0.15-μm InAlAs/InGaAs p-HEMTs.

devices, measured for 46 devices within the sample size of 4.8 mm $\times$ 3.2 mm, due to the higher etching selectivity of the ALET process. However, the slope efficiency S of the ALET device (98 mV/dec) was worse than that (93 mV/dec) of the RIE device, the reason for which is currently under investigation.

On-wafer S-parameter measurements were carried out from 500 MHz to 50 GHz. The IH$_{21}$I of the p-HEMTs as a function of the frequency is shown in Fig. 4. The extracted $f_T(f_{\rm max})$ is 233 GHz (167 GHz) for the ALET device and 203 GHz (175 GHz) for the RIE device. The improvement in f_T of the ALET devices is believed to result from the lower plasma-induced damage of the ALET, which was indirectly confirmed by the analysis of the transport property of the p-HEMT structures [11].

IV. Conclusion

The 0.15-μm InAlAs/InGaAs p-HEMTs have been fabricated using the ALET technology and the conventional RIE technology. The ALET technology yielded better electrical characteristics of InAlAs/InGaAs p-HEMTs, including transconductance, $I_{\rm ON}/I_{\rm OFF}$ ratio, DIBL, threshold voltage uniformity, and cutoff frequencies f_T, due to a much lower plasma-induced damage in the gate area and a higher etch selectivity of the ALET technology than the conventional RIE technology. The ALET technology shows potential for use in fabrication of high-performance and high-uniformity InGaAs/InAlAs p-HEMTs for integrated circuit applications.

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References

[1] T. Suemitsu, H. Yokoyama, Y. Umeda, T. Enoki, and Y. Ishii, "High-performance 0.1-μm gate enhancement-mode InAlAs/InGaAs HEMTs using two-step recessed gate technology," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1074–1080, Jun. 1999.

[2] T. Enoki, H. Ito, and Y. Ishii, "Reliability study on InAlAs/InGaAs HEMTs with an InP recess-etch stopper and refractory gate metal," *Solid State Electron.*, vol. 41, no. 10, pp. 1651–1656, Oct. 1997.

[3] G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni, "Improvement of DC, low frequency and reliability properties of InAlAs/InGaAs InP-based HEMTs by means of an InP etch stop layer," in *IEDM Tech. Dig.*, 1998, pp. 227–230.

[4] T. Suemitsu and M. Tokumitsu, "InP HEMT technology for high-speed logic and communications," *IEICE Trans. Electron.*, vol. E90-C, no. 5, pp. 917–922, 2007.

[5] T. Suemitsu, T. Enoki, H. Yokoyama, and Y. Ishii, "Improved recessed-gate structure for sub-0.1-μm-gate InP-based high electron mobility transistors," *Jpn. J. Appl. Phys.*, vol. 37, no. 3B, pp. 1365–1372, Mar. 1998.

[6] H. C. Duran, L. Ren, M. Beck, M. A. Py, M. Begerns, and W. Bachtold, "Low-frequency noise properties of selectively dry etched InP HEMTs," *IEEE Trans. Electron Devices*, vol. 45, no. 6, pp. 1219–1225, Jun. 1998.

[7] J. E. Maslar, J. F. Dorsten, P. W. Bohn, S. Agarwala, I. Adesida, C. Caneau, and R. Bhat, "Structural and electronic effects of argon sputtering and reactive ion etching on $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ studied by inelastic light scattering," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 13, no. 3, pp. 988–994, May 1995.

[8] R. Cheung, W. Patrick, I. Pfund, and G. Hahner, "Reactive ion etch-induced effects on 0.2 μm T-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP high electron mobility transistors," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 14, no. 6, pp. 3679–3683, Nov. 1996.

[9] T. R. Hayes, U. K. Chakrabarti, F. A. Baiochi, and A. B. Emerson, "Damage to InP and InGaAsP surface resulting from CH_4/H_2 reactive ion etching," *J. Appl. Phys.*, vol. 68, no. 2, pp. 785–792, Jul. 1990.

[10] S. D. Park, C. K. Oh, J. W. Bae, G. Y. Yeom, T. W. Kim, J. I. Song, and J. H. Jang, "Atomic layer etching of InP using a low angle forward reflected Ne neutral beam," *Appl. Phys. Lett.*, vol. 89, no. 4, pp. 043109-1–043109-3, Jul. 2006.

[11] S. D. Park, C. K. Oh, W. S. Lim, H. C. Lee, J. W. Bae, G. Y. Yeom, T. W. Kim, J. I. Song, and J. H. Jang, "Highly selective and low damage atomic layer etching of InP/InAlAs heterostructures for high electron mobility transistor fabrication," *Appl. Phys. Lett.*, vol. 91, no. 1, pp. 013110-1–013110-3, Jul. 2007.

[12] C. L. Lin, P. Chu, A. L. Kellner, H. H. Wieder, and E. A. Rezek, "Composition dependence of Au/$In_xAl_{1-x}As$ Schottky barrier heights," *Appl. Phys. Lett.*, vol. 49, no. 23, pp. 1593–1595, Dec. 1986.

[13] A. R. Saha, C. B. Dimitriu, A. B. Horsfall, S. Chattopadhyay, N. G. Wright, A. G. O'Neill, C. Bose, and C. K. Maiti, "Quantum-mechanical modeling of current–voltage characteristics of Ti-silicided Schottky diodes," *J. Appl. Phys.*, vol. 99, no. 11, pp. 113707-1–113707-3, Jun. 2006.

[14] D.-H. Kim, S.-J. Yeon, J.-H. Lee, and K.-S. Seo, "Performance enhancement of 0.13 μm $In_{0.65}GaAs$ pHEMTs by reduction of parasitic effect using novel double deck shaped (DDS) gate structure," in *IEDM Tech. Dig.*, 2003, pp. 723–726.

[15] D.-H. Kim, J. A. del Alamo, J.-H. Lee, and K.-S. Seo, "Logic suitability of 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs for beyond-CMOS applications," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2606–2613, Oct. 2007.