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Residual stress on nanocrystalline silicon thin films deposited under energetic ion bombardment by using internal ICP-CVD

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ABSTRACT

Nano/microcrystalline silicon thin films were deposited using an internal-type, inductively coupled, plasma-chemical vapor deposition (ICP-CVD) at room temperature by varying the bias power to the substrate. The structural characteristics of the deposited thin film were investigated. The deposition rate was increased by the application of a small RF bias power of 30 W (12.56 MHz), but was then decreased as the bias power was increased above 30 W. In addition, the application of bias power generally increased the residual compressive stress, which was attributed to the increased defect formation in the thin film due to the formation of interstitial atoms. The crystalline volume fraction was also decreased with increasing bias power. However, in the low bias power range of 0–60 W, the compressive stress in the deposited thin film was in the range of −34 to −77 MPa, which was lower than the residual stress in the range of −150 to −1050 MPa that is observed for the nano/microcrystalline silicon thin films deposited by capacitively coupled plasma.

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1. Introduction

Nano/microcrystalline silicon thin films are widely used in electronic and optical devices such as thin film transistors (TFT), solar cells, and image sensors [1]. Due to its higher carrier mobility than that of amorphous silicon film, nano/microcrystalline silicon has great potential in the fabrication of TFT-liquid crystal displays (TFT-LCD). In fabricating nano/microcrystalline silicon, crystallization by annealing is generally applied after the deposition of amorphous silicon by capacitively coupled, plasma enhanced, chemical vapor deposition (CCP-PECVD). In addition, annealing processes such as metal induced crystallization, metal-induced lateral crystallization, and excimer laser annealing are used to lower the crystallization temperature of amorphous silicon. However, these post-annealing techniques suffer some disadvantages such as high non-uniformity in crystallization, high cost, and metal contamination.

In fact, nano/microcrystalline silicon can be directly deposited with CCP-PECVD without annealing by using highly diluted SiH_4 gas mixtures and a high substrate temperature. However, the deposition rate is very low and the silicon deposited can be easily damaged due to the high plasma potential. Inductively coupled plasma (ICP) has a relatively high plasma density ($>10^{11}/cm^3$) [2,3] and a low plasma potential [4] that enable it to be used in the deposition of nano/microcrystalline silicon at a higher deposition rate and a low temperature. Among the various ICP sources, the internal-type ICP is known to be more applicable to extremely large area substrates such as TFT-LCD, so that its plasma characteristics have been extensively investigated by previous studies [5–8].

However, for the application of the internal ICP source to the deposition of nano/microcrystalline films of TFT-LCD, the deposited nano/microcrystalline silicon needs to possess adequate structural properties such as crystalline volume fraction [9], residual stress [10], grain size [11], and hydrogen bonding [12]. In this study, nano/microcrystalline silicon thin films were deposited on the glass or silicon substrate at room temperature using an internal-type ICP-CVD with a “double comb-type” antenna. Especially, the ion energy applied to the substrate was varied by applying a RF bias power to the substrate and the effect of this bias power on the structural properties of the deposited nano/microcrystalline silicon thin films was investigated in order to gain an understanding of the damage caused by ion bombardment during the deposition of the silicon thin film.

2. Experiment

A schematic diagram of the ICP-CVD system used in this experiment is shown in Fig. 1. The double comb-type ICP source was installed in a rectangular chamber having an inner size of 1020 mm × 830 mm. The double comb-type ICP antennas were composed of five sets of quartz-covered, linear Cu tubing that has an equal distance of about 15 cm. On one end of each linear antenna line, a 5 kW, 13.56 Mhz, rf power supply was connected alternatively through an L-type matching network while the other end of the antenna was connected to the

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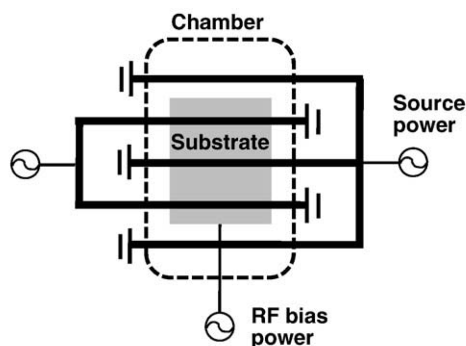

Fig. 1. Schematic diagram of the double comb-type, internal ICP-CVD used for deposition of nano/microcrystalline silicon thin films.

ground. The distance between the double comb-type antenna and the substrate was maintained at 10 cm. To deposit silicon thin films, Corning 1737 glass and a single-crystal silicon wafer were used. During the deposition, the substrate was biased by a separate 12.56 Mhz rf power supply and the bias power was varied from 0 to 240 W during the deposition. The rf power was fixed at 4 kW, while the SiH_4 concentration ($R=[SiH_4]/([He]+[SiH_4])$), total gas flow rate, and working pressure were maintained at 10%, 200 sccm, and 20 mTorr, respectively. Nano/microcrystalline silicon thin films with a thickness of about 350 nm were deposited at room temperature.

The crystallinity of the deposited nano/microcrystalline silicon thin films was investigated by using micro-Raman spectroscopy (InVia Basic Renishaw) with a 514 nm Ar^+ laser. A residual stress measurement tool (Frontier Semiconductor, FSM 500 TC) was used to determine the residual tensile or compressive stress in the films by measuring the changes of the substrate curvature using the Stoney's equation (ED you can use either "the Stoney equation" or "Stoney's equation"; please choose as you wish) before and after the deposition at room temperature [13,14]. The dark conductivity was calculated by using the current–voltage (I–V) characteristics of the deposited silicon thin films.

3. Results and discussion

Fig. 2 shows the deposition rate and dark conductivity of the deposited nano/microcrystalline silicon thin films as a function of RF bias power. An RF power of 4 kW at 13.56 MHz was applied to the ICP source and 0, 30, 60, and 240 W at 12.56 MHz to the substrate. A gas mixture of 200 sccm of He(90%)/SiH_4(10%) was used. As shown in the figure, the deposition rate of the nano/microcrystalline silicon thin films was initially increased by about 3% from 3.0 Å/s by application of a low RF bias power of 30 W. However, the deposition rate then continuously decreased with further increase of RF bias power. The initial increase of deposition rate was attributed to the increase in the surface activity and in the rate of surface reaction by increased low energy SiH_x^+ ion flux to the substrate, which increased the total flux to the substrate. However, when the RF power was further increased, the deposition rate was decreased by the sputtering effect resulting from the increased ion bombardment energy. The dark conductivity on the nano/microcrystalline silicon thin films decreased almost continuously with the addition and further increase of RF bias power, although this decrease was not significant. This decrease was related to the defects in the thin film, so that the application and increase of the RF bias voltage to the substrate increased the damage to the substrate due to the increased ion bombardment energy, similar to the case of increased plasma potential observed for CCP-PECVD, even without RF bias power.

Fig. 3 shows the Raman spectra of the deposited nano/microcrystalline silicon thin films as a function of Raman shift at different RF bias powers (ED note that the figure does *not* show the Raman spectra 'as a function of RF bias power'). The deposition condition of the nano/microcrystalline silicon thin films was the same as that in Fig. 2. The crystallization percentage and the amount of residual stress in the film can be calculated from the Raman spectra by the shift of the main peak position from that of single crystal silicon (520 cm^{-1}). As shown in the figure, the Raman peak position of the deposited nano/microcrystalline silicon thin films was close to 520 cm^{-1}, indicating the formation of crystalline silicon thin film. In addition, the slight shift of the Raman peak to a longer wave number (redshift) with increasing RF bias power revealed the increase of residual stress in the film.

Fig. 4 shows the full width at half maximum (FWHM) of the Raman spectral peak and the crystalline volume fraction calculated from the Raman spectra in Fig. 3, as a function of RF bias power. The Raman spectral peaks of the nanocrystalline silicon thin films were deconvoluted into three component peaks composed of two crystalline component peaks (*Ic* at 510, 520 cm^{-1}) and an amorphous component peak (*Ia* at 480 cm^{-1}). The volume fraction (*Xc*) of the crystallites in the nanocrystalline silicon thin films can be determined using the formula $Xc=(Ic_{510}+Ic_{520})/(Ic_{510}+Ic_{520}+y\,Ia_{480})$, where y

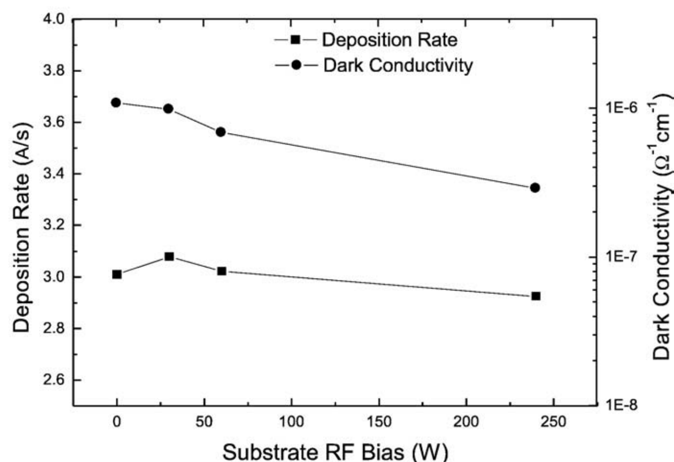

Fig. 2. Deposition rate and dark conductivity of the deposited nano/microcrystalline silicon thin films as a function of substrate RF bias power at room temperature.

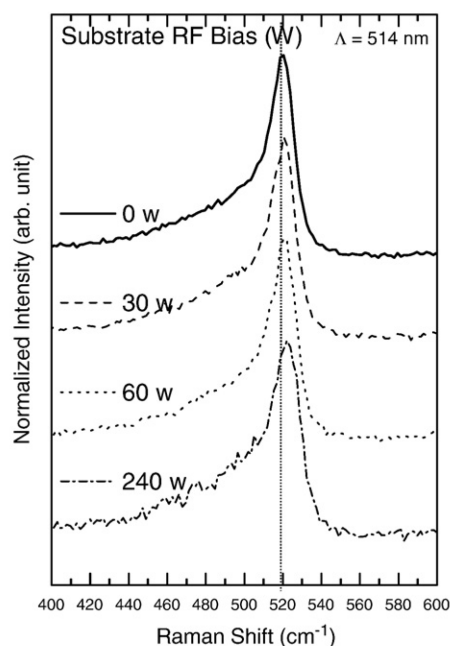

Fig. 3. Raman spectra of the deposited nano/microcrystalline silicon thin films as a function of Raman shift at various substrate RF bias powers at room temperature.

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is the ratio of the integrated Raman cross section for c-Si to a-Si [3]. As shown in the figure, the FWHM of the Raman spectral peak was steadily increased with increasing RF bias power from 17 cm^{-1} at no RF bias power to 23 cm^{-1} at 240 W of RF bias power, which indicated the decrease of crystallinity with increasing RF bias power due to the damage incurred by the deposited nano/microcrystalline silicon thin film. The increase of RF bias voltage decreased the estimated crystalline volume fraction slightly from 62% at no RF bias power to 58% at 240 W of RF bias power, possibly due to the damage to the nano/microcrystalline silicon thin films caused by the increased ion bombardment energy.

The redshift of the Raman spectral peak originated from the phonon confinement by the stress in the film [15]. The residual stress can be estimated from the Raman spectra by the following equation [16].

$$\sigma(\mathrm{MPa}) = -250\Delta\omega\left(\mathrm{cm}^{-1}\right) \tag{1}$$

In Eq. (1), σ is the in-plane stress and $\Delta w = w_s - w_0$, where w_0 is the optical phonon wave number of the stress free single crystal and w_s is the wave number of the stressed sample. Here, the negative and positive values of the residual stress show the compressive stress and tensile stress, respectively. As shown in Fig. 3, when the RF bias power was low (0–60 W), the redshift of the Raman peak from the crystalline silicon peak (520 cm^{-1}) was as low as 0.15–0.32 cm^{-1}, but it increased to 2.13 cm^{-1} when the RF bias power was increased to 240 W. The calculation of the residual stress using Eq. (1) enabled the compressive stress to be obtained as ranging from −37.5 MPa at no RF bias power to −532.5 MPa at 240 W of RF bias power; the result is shown in Fig. 5. The compressive residual stress obtained in the experiment and the increased compressive stress with increasing RF bias power were attributed to the formation of defects such as interstitial atoms in the nano/microcrystalline silicon thin films by the energetic ion bombardment.

Residual stress in a thin film can also be obtained by measuring the differences in the curvature of the substrate before and after the film deposition. The same thickness of nano/microcrystalline silicon thin films is deposited on silicon wafers and the differences in the curvature before and after the deposition are measured using a residual stress measurement tool. The radius of curvature of the substrate is determined from the slope of the straight line fitted to point by point subtraction data calculated from the before and after deposition scan data. The stress σ of silicon thin films can be

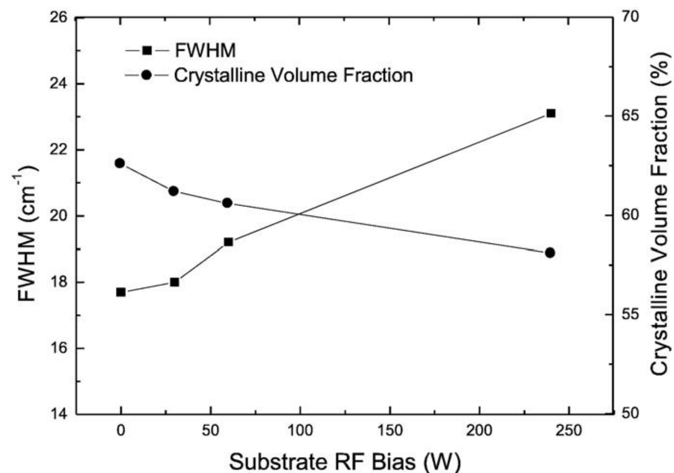

Fig. 4. FWHM and crystalline volume fraction of deposited nano/microcrystalline silicon thin films as a function of RF bias power at room temperature.

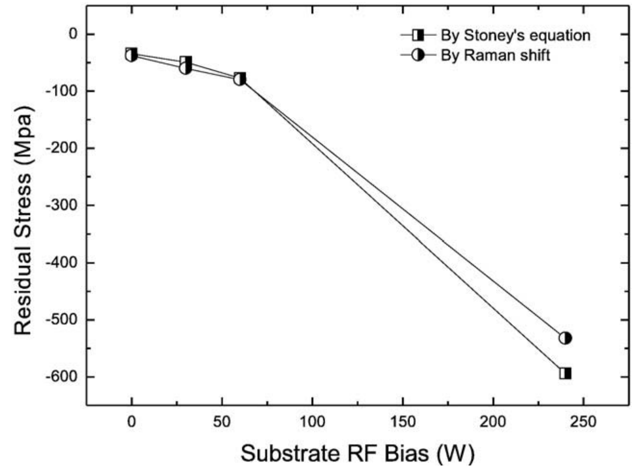

Fig. 5. Residual stress of deposited nano/microcrystalline silicon thin films as a function of RF bias power at room temperature. The residual stresses measured by a residual stress measurement tool using Stoney's equation and estimated by the Raman spectral redshift are shown.

determined by the curvature of the substrate according to the Stoney's equation [13,14].

$$\sigma = \frac{ED^2}{6(1-v)tR} \tag{2}$$

where E is the Young's modulus of the substrate, D the thickness of the substrate, v the Poisson's ratio of the substrate, $t$the film thickness, and R the radius of curvature change. The calculated residual stress, shown in Fig. 5 as a function of RF bias power, was increased from −34.43 MPa at no RF bias power to −594.3 MPa at 240 W of RF bias power; this increase almost similar to the residual stress estimated by the Raman spectral peak shift. According the results by Paillard et al. [15], the residual stress of the crystalline silicon thin films deposited by CCP-CVD (PECVD) without RF bias power shows a compressive stress in the range from −150 to −1050 MPa [17]. In comparison, the residual stress obtained in our experiment by internal-type ICP-CVD at low RF bias powers (0–60 W) was significantly lower than those obtained by CCP-CVD. The lower residual stress obtained in our experiment, even with a RF bias power, was attributed to the lower plasma potential obtained in the ICP-CVD system.

4. Conclusions

In this study, nano/microcrystalline silicon thin films were deposited using an internal-type, ICP-CVD system at room temperature with a gas mixture of He(90%)/SiH_4(10%) as a function of RF power applied to the substrate in addition to the RF power applied to ICP source. The structural properties of the deposited thin films, such as crystalline volume fraction and residual stress, were investigated to study the degree of physical damage caused by ion bombardment. The application of a small RF bias power to the substrate slightly increased the deposition rate by about 3%, possibly due to the increase of SiH_x^+ ion flux to the substrate. However, further increase of the RF bias power decreased the deposition rate due to the sputtering effect caused by the increased ion bombardment energy. The increased RF bias power decreased the crystallization volume fraction but increased the residual compressive stress in the deposited thin film. The decreased crystalline volume fraction and the increased residual compressive stress with increasing RF bias power were related to the substrate damage incurred by the increased ion bombardment energy. However, the residual stress measured at low RF bias power was generally lower than that of crystalline silicon thin films obtained by

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CCP-CVD without RF biasing, possibly due to the low plasma potential that reduced the ion bombardment energy.

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