A Novel Damage-Free High-k Etch Technique Using Neutral Beam-Assisted Atomic Layer Etching (NBALE) for Sub-32nm Technology Node Low Power Metal Gate/High-k Dielectric CMOSFETs

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Abstract

For the first time, a novel damage-free neutral beam-assisted atomic etching process has successfully demonstrated the removal of the residual high-k dielectric layer after gate patterning. Due to its neutralized atomic flux and chemical reaction, high etch selectivity is observed to improve device performance and reliability. This process should significantly enhance high-k/metal gate manufacturability.

1. Introduction

Since the physical thickness of SiON has been aggressively scaled, plasma-induced damage (PID) because of increased gate leakage has not been a problem [1]. However, PID has been observed in aggressively scaled high-k gate dielectrics (EOT < 1.0 nm), attributed to the greater physical thickness of the high-k layer leading to more charge trapping as shown in Fig. 1 [2].

In high-k/metal stack formation, a wet- or dry-based cleaning process is used to remove residual high-k dielectric with minimal substrate damage. A previous study reported that a dry etch and an HF-based wet etch can cause PID and undercut of the high-k dielectric at the gate edge region, respectively [3]. The recessed high-k structure during a wet etch process shows significant gate edge leakage current due to the leakage path formed in the heterogeneous interface between the high-k dielectric and the nitride capping layer.

In conventional SiON with poly-Si gate stack devices, the gate is reoxidized to anneal out the PID and to round the gate bottom edge profile to reduce the vertical field [3,4]. Due to the oxidation of the metal and growth of the interfacial layer, however, this conventional gate re-oxidation process cannot be used for a high-k/metal stack. In previous studies, a low temperature plasma oxygen treatment was demonstrated to encapsulate/passivate the gate edge leakage path in a high-k/metal stack, but the process repeatability and uniformity is still in question [4,5].

For residual high-k removal after gate patterning, therefore, a damage-free and highly selective dry etching process is necessary. Accordingly, for the first time, we have demonstrated a novel neutral beam-based atomic layer etching process for metal gate/high-k dielectric CMOSFET integration.

2. Experiment

The neutral beam system consists of a plasma source, grid system, and neutralizer as shown in the schematic in Fig 3. The ion beams extracted from the plasma source are neutralized when the beam goes through the neutralizer. Fig. 4 displays the current density (J_G) as measured by a Faraday cup as a function of the acceleration voltage of gas without and with the neutralizer. With the neutralizer, the neutralization rate was over 90% based on the beam current measurement. Based on this neutral beam (NB) system, atomic layer etching (ALE) can be performed through a sequence of adsorption-desorption steps. During ALE, the chemisorbed chlorine compound is removed by the irradiation from an energetic Ar beam.

To verify the NBALE process in CMOS integration, high-k/metal electrode CMOSFETs were fabricated using 45 nm CMOS technology (Fig. 5). HfO_2 3 nm thick was deposited using atomic layer deposition (ALD) with poly-Si/TiN as the gate electrode. Equivalent oxide thickness (EOT) was extracted from measured capacitance-voltage (CV) curves using the North Carolina State University (NCSU) CVC model. Mobilities were extracted from W/L = 10 μm/1 μm devices using the NCSU mob2d model.

3. Results and Discussion

To confirm the end-point of the high-k removal, X-ray photoelectron spectroscopy (XPS) measurements after ALE were performed as shown in Fig 6. The Hf peak disappeared after 35 cycles of the ALE high-k removal process, indicating complete removal of the high-k. Minimal loss of the bottom interfacial SiO_2 was confirmed by transmission electron microscopy (TEM), which suggests that NBALE-based high-k etching exhibits a high etch selectivity (Fig. 7). In addition, the low RMS results from atomic force

microscopy (AFM) suggest that our NBALE will provide a wide process window in terms of surface roughness (Fig. 8).

No changes in the EOT values and bulk dielectric properties were observed from MOSCAP C-V and I-V curves (see Fig. 9 and 10), which results in similar mobility (Fig. 11). Due to the neutralized beam treatment, however, interface trap density (N_{it}) is less than the control plasma etch (PE) process (Fig. 12). These results are expected because they represent the area properties of the gate dielectric and the NBALE is helpful in mitigating PID, high-k undercut, and surface damage. In a given EOT range, PID-induced device parameter shifts are negligible [2]. Therefore, we need to focus on how high-k undercut and perimeter damage affect device characteristics.

When the gate length (L_{gate}) is decreased, three sample devices show different threshold voltage (V_{th}) roll-off behavior as shown in Fig. 13. A reverse short channel effect (RSCE) is observed in the control PE and Wet etch samples and the RSCE in the NBALE device can be ignored. The causes of RSCE can be non-uniform channel doping by halo implant, additional charge build-up at the gate edge during gate formation step, and an increase in local EOT at the gate edge. Since all samples were processed using the same implantation conditions, we can rule out the channel non-uniformity. The greatest V_{th} roll-up is observed with the wet etched samples, which is due to the localized EOT increase by the low-k SiN fill in the high-k undercut. The moderate RSCE in the dry etched samples is attributed to the additional charge build-up caused by gate edge damage. For the NBALE samples, the negligible V_{th} roll-up resulted from less high-k undercut and charge build-up. The inset of Fig. 13 exhibits normalized I_{off} uniformity. The NBALE samples show the best uniformity among all the samples due to the mitigated PID and high-k undercut.

From I_d-V_g curves in Fig. 14, low field gate leakage was dramatically improved with the NBALE process. It is caused by the low edge damage and high-k undercut from employing neutral beam-assisted ALE. This edge leakage improvement is confirmed by gate leakage current behavior in a perimeter-intensive MOS capacitor pattern as shown in Fig. 15. Again, ALE devices have less gate leakage (I_{gate}) at a low gate bias due to the damage-free and conformal high-k removal. When L_{gate} is decreased, the gate leakage becomes greater for PE samples while J_{gate} is almost the same for ALE samples (Fig. 16). When the channel length becomes shorter, the perimeter leakage component and the leakage variation become greater with the dry etch. Because of less PID in ALE, transconductance (G_m) and G_m variation were improved compared to the PE (Fig. 17). Due to its low perimeter leakage and high uniformity, ALE samples show improved I_{on}-I_{off} characteristics, especially improved I_{off} variation at a given I_{on} (Fig. 18).

Device characteristics need to be checked using an antenna structure to ensure that the NBALE is damage-free. V_{th} and G_m variations in antenna structures are shown in Fig. 19. Due to the charging effects in PE-based high-k removal, V_{th} increases 50 mV and G_m degrades in the antenna structures. Even with an area type of antenna, G_m degradation was significant with the PE process, suggesting that PID causes interface state generation as shown in Fig. 12. It is expected that PE will degrade reliability characteristics.

The ALE process exhibits improved positive bias temperature instability (PBTI) behavior as shown in Fig. 20. This is possibly due to less exposure to ionic charging during the neutral beam process and thus lower N_{it} compared to PE. This PBTI is directly related to the areal dielectric degradation. To investigate gate edge effects, a hot carrier stress test was performed since accelerated carriers inject at the gate edge. Again, ALE devices showed less V_{th} shift due to less perimeter damage (Fig. 21 and 22).

4. Conclusions

A novel neutral beam-based atomic etching process successfully demonstrated removal of the residual high-k dielectric layer after gate patterning. Due to its unique system configuration, the PID-free/high selectivity high-k removal process results in lower gate leakage than the control. We believe the ALE process is a promising technique for sub-32 nm integration, especially for low power applications.

Acknowledgements

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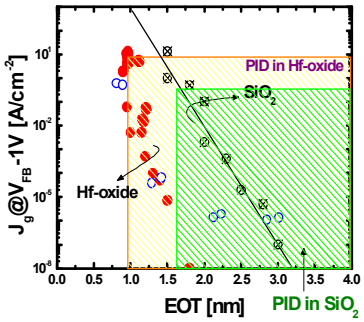


Fig 1. Plasma-induced damage (PID) trends. Previously the PID of aggressively scaled high-k gate dielectrics (EOT < 1.0 nm) was studied in metal gate/high-k dielectric CMOSFETs [2].

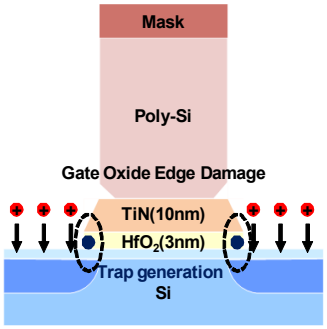


Fig 2. The plasma-induced damage (PID) mechanism. Plasma etching of gate oxide could cause gate oxide edge damage. Neutral beam etching could be a solution.

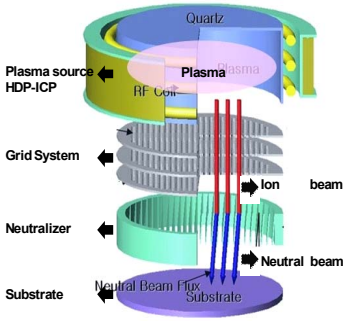


Fig 3. Schematic diagram of a neutral beam etching system consisting of a plasma source, grid system, and neutralizer. The neutral beam was generated by surface neutralization of the ion beam.

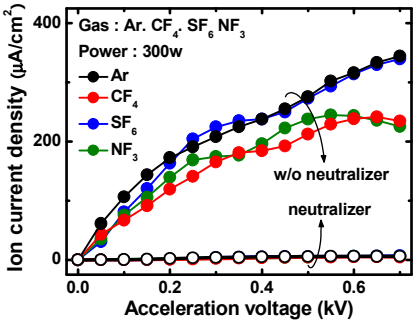


Fig 4. Ion current density (J_G) measured by a Faraday cup as a function of gas with or without a neutralizer. The neutralization rate was over 90%.

- Isolation & Well formation
- Gate Stack Formation

	Poly-Si /TiN	Dielectric	HfO_2	EOT
1	PE	WE	3nm	1.23nm
2		PE		1.2nm
3		ALE		1.2nm

- N & P LDD/halo I/I
- Nitride spacer
- N & P SD I/I
- SD RTA ILD & Contact formation
- Metallization & Forming Gas Anneal (480ºC, 30min)

Fig 5. Process flow of CMOS fabrication.

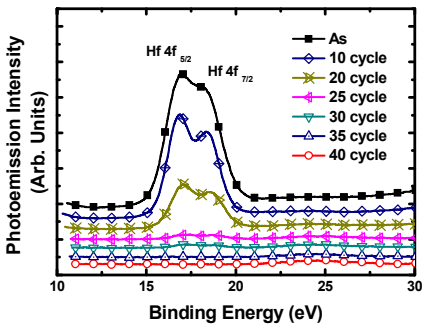
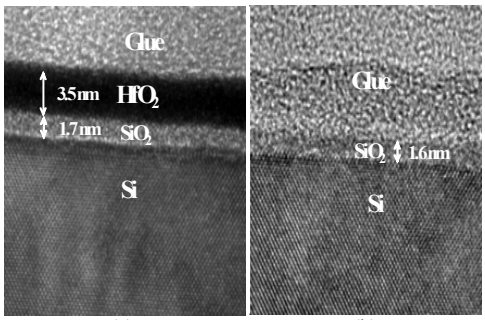
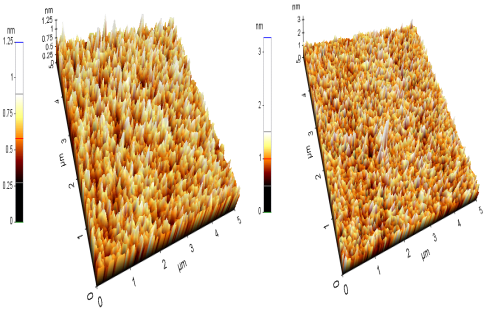


Fig 6. Hf peak in XPS as a function of the ALE cycle. The Hf peak disappeared after 35 cycles of the ALE high-k removal process.



(a) (b)

Fig 7. TEM of (a) reference (b) atomic layer etching (ALE) of gate oxide in metal gate/high-k dielectric CMOSFETs.



(a) (b)

Fig 8. AFM results of (a) PE (RMS = 3.2) and (b) ALE (RMS = 1.63).

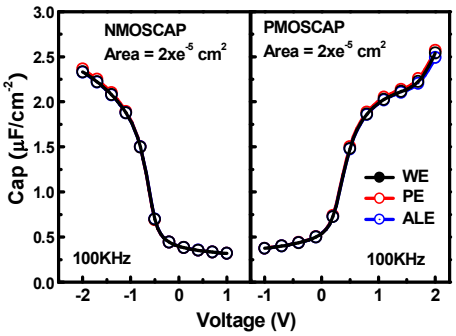


Fig 9. C-V measured in (a) NMOSCAP and (b) PMOSCAP with an area of 200 μm^2.

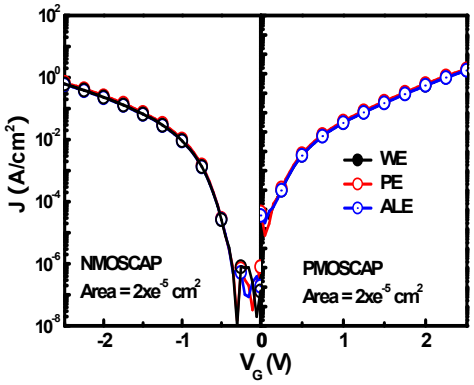


Fig 10. I-V measured in (a) nMOSCAP and (b) pMOSCAP with an area of 200 μm^2.

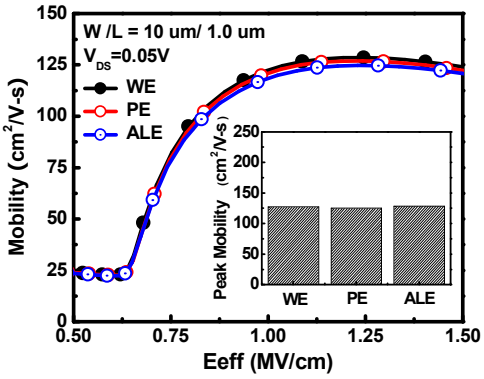


Fig 11 High field electron mobility measured in nMOSFET with a 10 μm wide and 1 μm long gate is similar for PE and ALE.

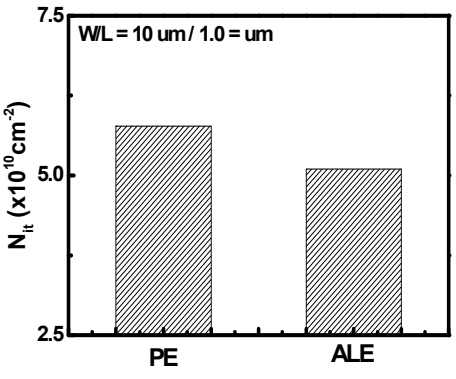


Fig. 12. N_{it} measured in nMOSFETs. Due to the neutralized beam treatment, interface trap density (N_{it}) was better than the control plasma etching (PE) process.

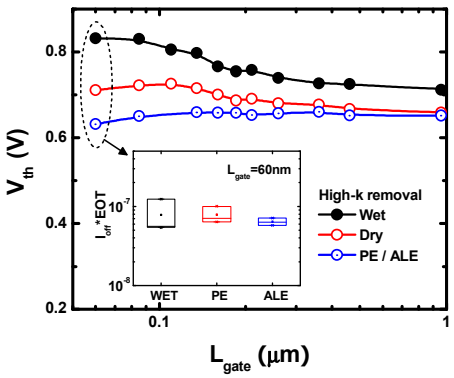
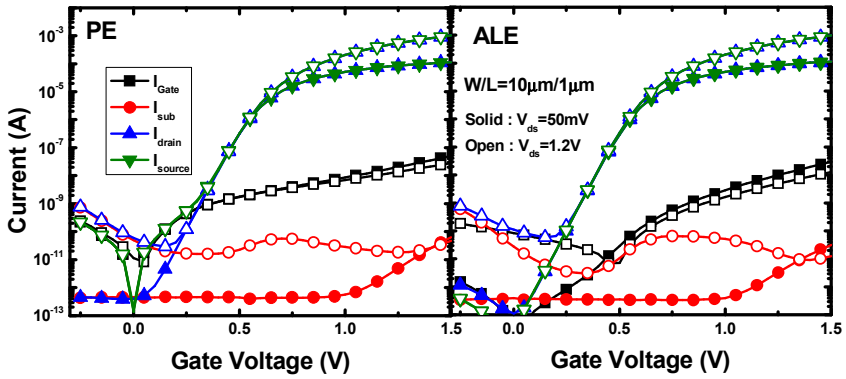


Fig 13. V_{th} measured in nMOSFET for gate lengths from 1 μm to 60 nm.



(a) (b)

Fig 14. I_dV_g characteristics for (a) PE and (b) ALE process. Low field I_{gate} improved in the ALE sample.

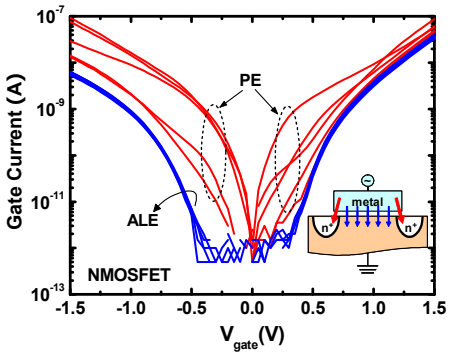


Fig 15. Peri-leakage curves for PE and ALE. Due to less gate edge damage, the low field I_{gate} decreased with ALE.

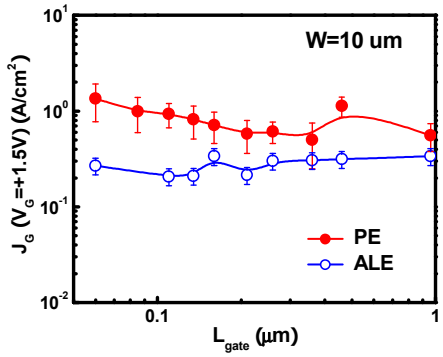


Fig 16. Due to PID during high-k removal, the perimeter leakage becomes greater for PE samples.

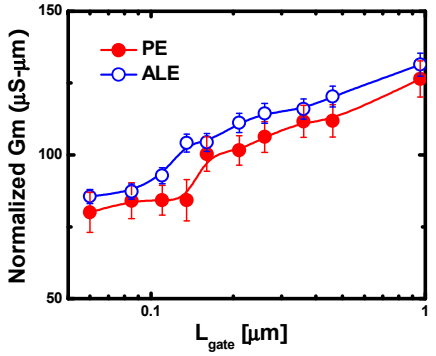


Fig 17. Due to less PID with ALE, transconductance improved compared to PE.

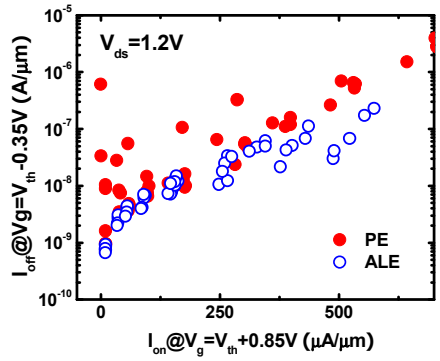


Fig 18. I_{on}-I_{off} measured in nMOSFETs. I_{on}-I_{off} improves in the ALE samples compared to the PE cases due to improved gate edge damage.

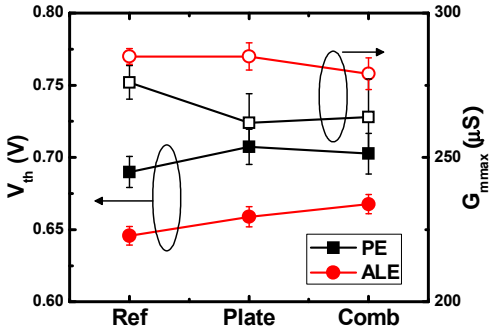


Fig. 19. V_{th} and G_m variation in an antenna structure. Due to the charging damage in PE, V_{th} increased by 50 mV and G_m degraded.

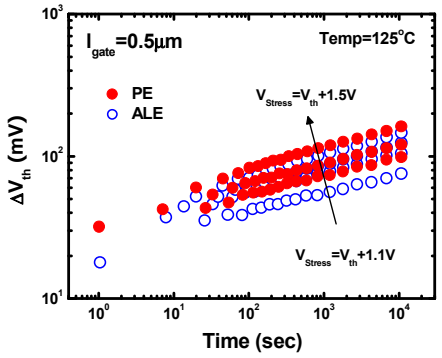


Fig 20. Comparison of ΔV_T under PBTI (V_{Stress} = V_G + 1.1 V/1.3 V/1.5 V) measured in a 0.5 μm long nMOSFET at 125°C.

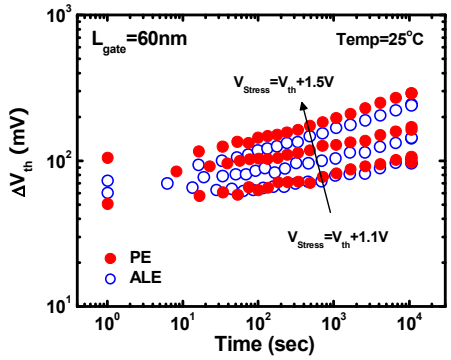


Fig 21 Comparison of ΔV_T under HCI (V_{Stress} = V_G + 1.1 V/1.3 V/1.5 V, V_D = V_{Stress}) measured in a 60 nm long nMOSFET at 25°C.

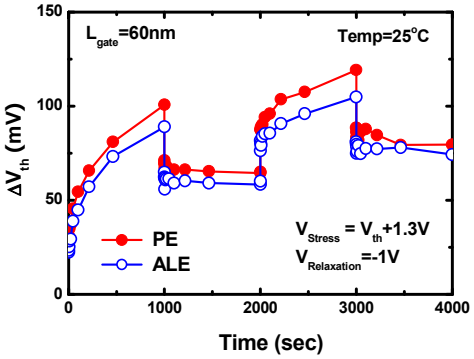


Fig 22. Comparison of ΔV_{th} stress and recovery rate under HCI (V_{Stress} = V_G + 1.3 V, V_D = V_{Stress}, and $V_{Relaxation}$ = -1 V).