Fabrication of InAs composite channel high electron mobility transistors by utilizing Ne-based atomic layer etching

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High electron mobility transistors (HEMTs) with InAs/InGaAs composite channel were fabricated by employing low damage, highly selective Ne-based atomic layer etching (ALET) for the dry gate recess process. Ne-based ALET exhibited very high etch selectivity of InP over InAlAs which is suitable for dry gate recess process removing InP etch stop layer on top of InAlAs Schottky barrier layer. The plasma induced damage on the exposed InAlAs surface due to the ALET was much lower than that due to the conventional Ar-based reactive ion etching (RIE), which was verified by atomic force microscopy and Hall measurements. For further comparison, dc characteristics were compared for the two types of 0.3 μm HEMTs fabricated by utilizing ALET and conventional RIE during the dry gate recess processes. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2780113]

InP-based high electron mobility transistors (HEMTs) have shown remarkable performance improvement over the last two decades. Currently, very high unity-current-gain cutoff frequency (f_T) of 562 GHz was demonstrated by 25 nm gate pseudomorphic InGaAs HEMTs.[1] The relentless gate-length scaling down to sub-100-nm brought stable metal-gate forming technology into the center of the research activities on nano-HEMTs. The gate formation in InP-based HEMTs requires nanopatterning highly controllable gate recess etching. Electron-beam lithography has been conventionally utilized to realize e-beam resist profile suitable for *T*-gate formation by using trilayer e-beam resist systems. Gate recess technology is one of the key technologies determining device performances because it influences the Schottky gate diode characteristics and the vertical distance from channel to the gate metal. Wet gate recess process has been utilized to manufacture InAlAs/InGaAs HEMTs with highly selective succinic-acid based etch chemistry.[2,3] Etch stop layers such as AlAs and InP have also been used to achieve uniform device characteristics.[4–6] InP etch stopper was developed by molecular beam epitaxy together with metal-organic chemical-vapor deposition. InP is lattice matched to the device heterostructures consisting of InAlAs/InGaAs/InP so that there is no strain in the heterostructures. When InP layer was inserted in the layer structures, dispersion and kink effect were alleviated because the thin InP layer effectively passivated the InAlAs layer. However, InP is known to have lower Schottky barrier height ($\Phi_B = \sim 0.3$ eV) which leads to excessive gate leakage current and thus low breakdown behavior when gate electrode is formed on top of InP layer.[7,8] As InP layer became popular in the layer structures of HEMTs, it is required to selectively remove InP layer on top of InAlAs layer. Even though there is wet etch chemistry that can remove InP selectively on top of InAlAs layer, it is not suitable for gate recess process because its etch rate is too high that lateral etching could not be easily controlled. The only available technology to remove InP etch stop layer on top of InAlAs layer is the reactive-ion-etching (RIE)-based dry recess technology. Ar-based reactive ion etching was developed for dry recess process, but its etch selectivity is limited and the plasma induced damage is also indispensable during the device fabrication process. Suemitsu *et al.*[6] proposed the two-step-recess technology, in which the selective wet etching was utilized to remove the highly doped capping layers consisting of *n*+ InGaAs and *n*+ InAlAs and the following Ar-based plasma etching was utilized to remove the InP etch stop layer. By forming Schottky gate diode on top of InAlAs after removing InP etch stop layer, the breakdown voltage of the devices was considerably improved. However, Ar-based plasma RIE exhibited finite etch selectivity between InP and $In_{0.52}Al_{0.48}As$ ($\sim$18) and it induced significant damage to the surface of $In_{0.52}Al_{0.48}As$ due to the use of energetic reactive ions. It includes the structural disruption, the stoichiometric modification, and the surface roughness increment.[9–12] Recently, Park *et al.* demonstrated Ne-based atomic layer etching (ALET), which exhibits excellent etch selectivity and maintains good surface stoichiometry on the exposed InAlAs layer. The ALET-based dry gate recess process is promising in terms of manufacturing uniform device characteristics and low damage high quality gate metallizations.[13,14]

In this letter, the impact of ALET on the structural and electrical transport properties of InAlAs/InGaAs heterostructures was investigated by comparing the surface roughness and electrical characteristics of the HEMT heterostructures etched with ALET and conventional RIE. For the device applications, 0.3 μm InAlAs/InGaAs HEMTs were

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fabricated by utilizing two types of dry recess technologies employing ALET and RIE and their electrical performances were compared.

The device heterostructures utilized in this study were grown by molecular beam epitaxy on top of a 500-nm-thick $In_{0.52}Al_{0.48}As$ buffer layer prepared on a 3 in. semi-insulating InP substrate. The detailed device structures from the bottom to the top consist of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ (4/6/4 nm) InAs composite channel, 3-nm-thick $In_{0.52}Al_{0.48}As$ spacer, Si δ-doping plane, 8-nm-thick $In_{0.52}Al_{0.48}As$ Schottky layer, 6-nm-thick InP etch stop layer, and 35-nm-thick highly doped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ cap layers.

To investigate the impact of etching methods on the surface morphologies of the etched HEMT heterostructures, atomic force microscopy (AFM) studies were carried out on the exposed InAlAs Schottky layer. The multilayer cap was removed by selective citric-acid based wet etch, and InP etch stop layer was removed by three separately optimized etching processes such as selective wet etch, conventional RIE, and ALET. For the selective wet etching of 6-nm-thick InP etch stop layer, the HCl-based solution was utilized. Conventional RIE process conditions include working pressure of 10 mTorr, Ar of 50 SCCM, and rf power of 7 W in Oxford Plasma Lab-80 chamber. The detailed process condition can be found in Ref. 14. The etch rates of InP were 160 Å/min, 4 Å/min, and 1.47 Å/cycle by wet etch, RIE, and ALET, respectively. The selectivities of InP over InAlAs were found to be 55, 10, and 70 for wet etch, RIE, and ALET, respectively.

The rms surface roughness values measured by AFM were 7.7, 2.9, and 1.37 Å for the samples prepared by HCl-based wet chemical etch, RIE-based pure physical sputter etch, and ALET, respectively. The surface roughness obtained from the wet etched sample can be ascribed to the presence of interstitial layer at the interface of InP and InAlAs,[15] and it is higher than the surface roughness induced by physical damage during the sputtering process and during Ar-based RIE process. The smallest rms roughness obtained from ALET is due to the combinational etching mechanism of chlorine-based chemical etching and physical Ne sputtering. Neither spontaneous etching of InP by Cl_2 nor pure physical sputter etching of InP by the low energy ($<$27 eV) Ne neutral beam irradiation can occur during the neutral beam ALET process.[14] InP etching takes place only when Cl_2 and neutral Ne beam are sequentially supplied. The etch rate is self-limited to 1 ML/cycle because the chloride is formed only on the surface layer and only the chlorides are etched during the neutral beam irradiation. By localizing chemical reaction only at the surface by adsorbing Cl_2 on to InP surface and by minimizing the energy of Ne beam, the smallest rms surface roughness could be achieved by ALET. The smallest rms roughness and high etch selectivity obtained from ALET warranting the best gate diode characteristics, process repeatability, and device uniformity prove that the ALET is very promising technology for gate recess process for HEMTs.

A van der Pauw Hall structure, with an active area of 100×100 μm^2, was fabricated to measure Hall mobility ($\mu_{n,\mathrm{Hall}}$) and sheet carrier density (n_s). Selective wet etch, Ar-based conventional RIE, and ALET techniques were utilized to etch 6-nm-thick InP etch stop layer during the gate patterning process.

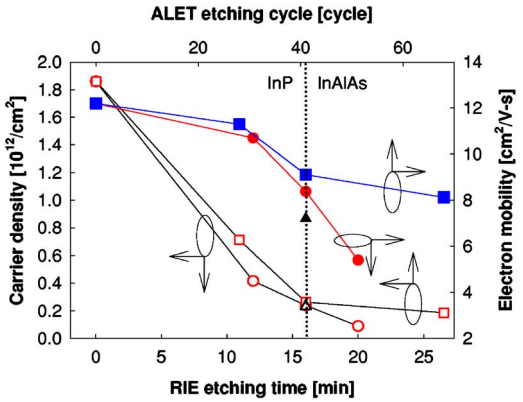

FIG. 1. (Color online) van der Paw Hall measurement results. Hall mobility and sheet carrier density are plotted as functions of total etching cycle for ALET and total etching time for RIE, respectively. (■) and (□) represent electron mobility and sheet carrier density of atomic layer etched sample. (●) and (○) represent electron mobility and sheet carrier density of relative ion etched sample. (▲) and (△) represent electron mobility and sheet carrier density of wet etched sample.

In Fig. 1, the measured Hall mobility and sheet carrier density are plotted as functions of total etching cycles for ALET and total etching time for RIE, respectively. Measurement results after removing InP by selective wet etching are also included in the figure. The critical point where InP was completely removed is marked with a vertical dotted line. It corresponds to 16 min and 41 cycles for RIE and ALET, respectively. The critical point was determined by measuring the etch depth by utilizing AFM. For easier comparison, the scales of bottom and top x axes were carefully determined so that the critical point coincides at the same place. Although the n_s and $\mu_{n,\mathrm{Hall}}$ significantly decrease as the total etching time of RIE increases even after the critical point, this phenomenon is not severe in the samples etched with ALET. It can be ascribed to the continuous etching of InAlAs due to the nonideal etch selectivity of RIE process and the physical and electrical damages on the exposed InAlAs layer. When the InAlAs layer is thinned down due to the nonideal etch selectivity, the carrier density decreases by the surface depletion. The plasma induced damage on the exposed InAlAs layer leading to roughened surface increases the carrier scattering resulting in the decreased Hall mobility. For the further investigation of plasma induced physical damage, an angular resolved x-ray photoelectron spectroscopy was utilized to analyze the stoichiometric modification of $In_{0.52}Al_{0.48}As$ surface. No significant change of the surface composition was observed after the ALET, while significant decrease in the ratios of Al/In and As/In was observed in the case of RIE after the plasma etching,[14] which will be described later. Finally, we applied the developed ALET technology to the fabrication of the 0.3 μm composite channel InAs HEMTs. The fabrication process for the HEMT began with mesa isolation down to the InAlAs buffer layer by a wet chemical etching. The multilayer Ohmic metallization of Ni/Ge/Au (10/45/200 nm) was e-beam evaporated and annealed at 275 °C for 45 s under a nitrogen environment. The resulting specific Ohmic contact resistivity was measured to be as low as 0.03 Ω mm. The coplanar pad patterns for ground-signal-ground rf probing were photolithographically defined and Ti/Au (20/300 nm) metallization was evaporated and lifted off. Double exposure technique was utilized to delineate 0.3 μm T-gate pattern on trilayer e-beam resists

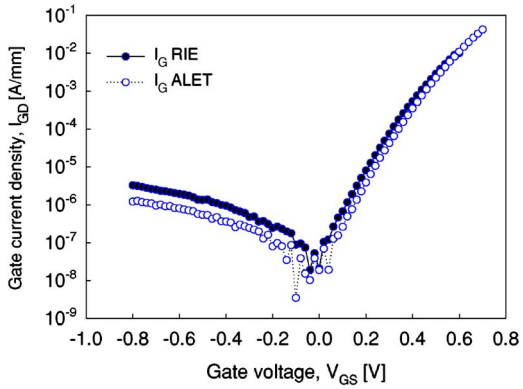

FIG. 2. (Color online) dc *I-V* characteristics of the Schottky gate diode after the ALET and RIE of plasma.

(ZEP520A/PMGI/ZEP520A). Subsequently, gate recess was carried out by utilizing a two-step gate recess which is the combination of wet etch of the *n*-InGaAs/*n*-InAlAs cap layer by citric based wet solution and dry etch of InP etch stop layer. For comparison, the conventional RIE and ALET processes were utilized for dry etching. The gate metallization consisting of Ti/Pt/Au (20/20/300 nm) was evaporated and lifted off. Figure 2 shows the gate diode characteristics of 0.3 μm HEMTs fabricated by using RIE- and ALET-based dry gate recess processes. The gate diodes fabricated with the ALET exhibited better electrical characteristics than the diodes fabricated with conventional RIE in terms of leakage current, Schottky barrier height (Φ_B), and ideality factor (η). The ALET device shows the lower ideality factor and the higher Schottky barrier height (η=1.6 and Φ_B=0.54 eV) than RIE device (η=1.8 and Φ_B=0.37 eV). The Schottky barrier height and ideality factor were measured by using a standard *I-V* technique. The lower ideality factor obtained from the devices fabricated by using the ALET is believed to be due to the lower physical damage on the $In_{0.52}Al_{0.48}As$ surface by the ALET compared with that by the conventional RIE. The Schottky barrier height of the devices fabricated by conventional RIE is much lower than that of the devices fabricated by ALET. It is due to the stoichiometric change on the exposed InAlAs Schottky layer by conventional RIE, which was verified by the x-ray photoelectron spectroscopy study on the etched surface. The Al/In ratio on the InAlAs surface exposed by ALET (0.87) was essentially the same as bulk Al/In ratio (0.92), but it changed to 0.3 for the conventional RIE. When the aluminum content in the $In_xAl_{1-x}As$ decreases, the Schottky barrier height will be reduced.[16]

Figure 3 shows typical transfer characteristics of the

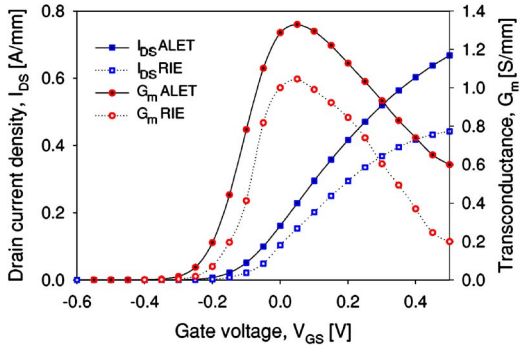

FIG. 3. (Color online) Transfer characteristics of the 0.3 μm two-step gate recess HEMTs fabricated by utilizing ALET and RIE.

HEMTs fabricated by RIE (device R) and those fabricated by ALET (device A). Device A shows the higher transconductance ($G_{m,\max}$=1.33 S/mm) than device R ($G_{m,\max}$=1.04 S/mm). It is due to the higher source access resistance of device R (0.27 Ω mm) than that of device A (0.24 Ω mm) and the worse gate modulation characteristics of device R, which can be ascribed to the higher plasma damage induced by conventional RIE process. The device processed with RIE exhibits more positive threshold voltage than that with ALET, which can be explained by thinner InAlAs Schottky layer leading to the severe surface depletion, which was verified by cross-sectional transmission electron microscope study. The InAlAs thickness of the devices fabricated by RIE was 15 Å thinner than that of the devices fabricated by ALET. It is ascribed that the surface roughness induced at the InAlAs layer is much higher in device R than in device A, which was verified by AFM study earlier.

In conclusion, we have demonstrated the fabrication of HEMTs by utilizing ALET-based gate recess process. The two dry gate recess processes such as conventional RIE and ALET were employed to fabricate 0.3 μm HEMTs and their performances were compared. The devices fabricated with ALET technology demonstrated better Schottky gate diode characteristics and better Hall mobility. The benefits of the ALET technology were the better etch selectivity of InP against the underlying $In_{0.52}Al_{0.48}As$ layer and much less plasma induced damage when it is compared with conventional RIE.

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